JEDEX 2003

Memory Futures
Track 2
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"High Speed Digital Systems Require Advanced Probing Techniques for Logic Analyzer Debug"

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Objective

1) **Predict the electrical effect of a Logic Analyzer Probe on the target**

2) **Predict the electrical effect of the target on the Logic Analyzer Probe**

3) **Discuss a common probing technique (Stub Probing)**

4) **Present modern Logic Analyzer Probing Solutions**

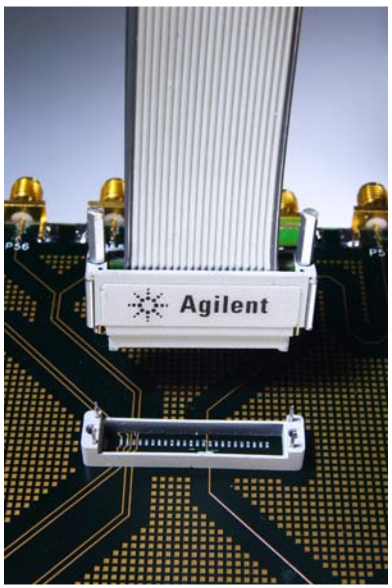
- **General Purpose**
- **Memory System Specific**

The Logic Analyzer

- A logic analyzer is a piece of general purpose, test equipment
- It provides debug/validation for digital systems
- It is connected to the target system using a probe

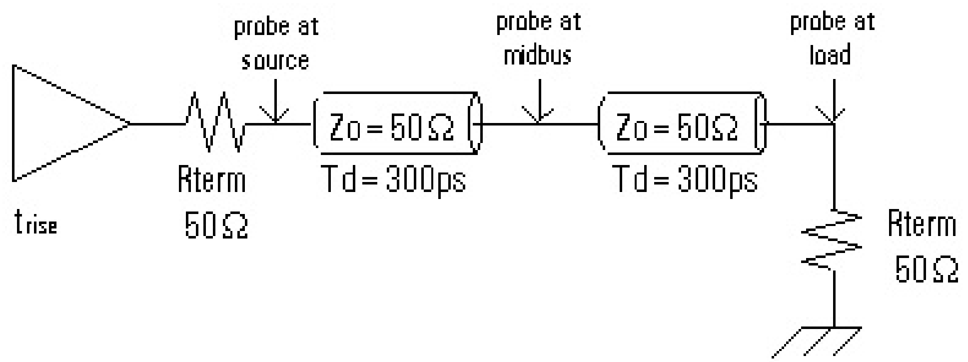
The Probe

- The "electrical" connection from the target to the analyzer
- The "mechanical" connection from the target to the analyzer
- Both are important factors in selecting a probe



Electrical Considerations of a Probe

- Electrical Loading on the Target System
- Signal Quality at the Tip of the Probe



- The Topology of the Target System Affects Both
- The Location of the Probe Affects Both

How can we Predict the Affect of the Probe?

- Logic Analyzer Vendors provide electrical specifications about the probes:

  - Equivalent Load Models (SPICE Decks)

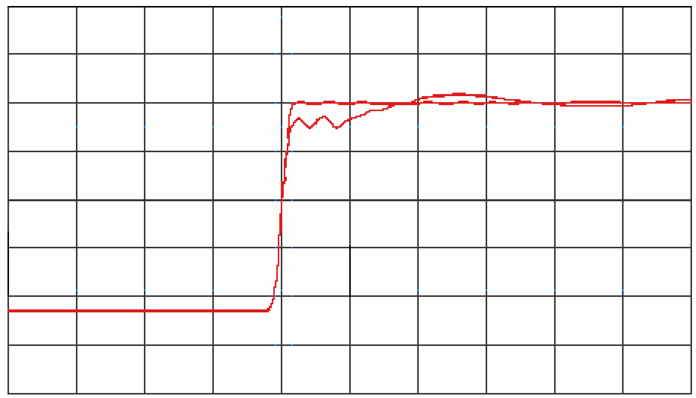
  - Equivalent Lumped Capacitance

  - Impedance Profiles

  - Maximum Data Rates / Minimum Amplitudes

SPICE Simulation

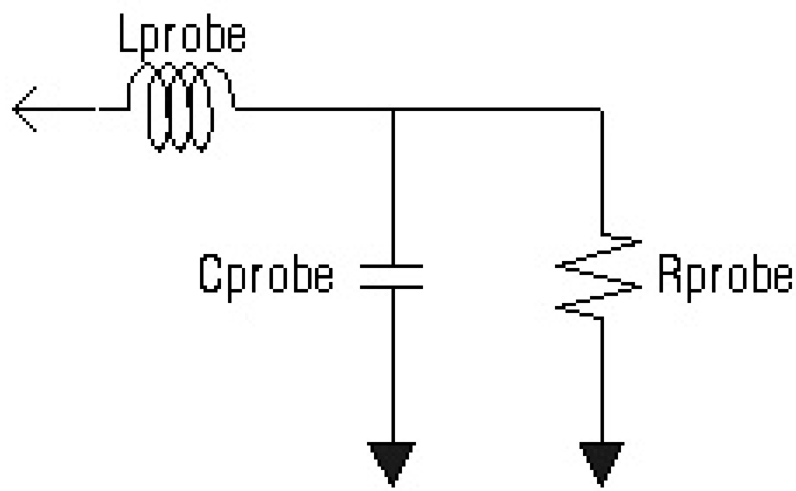
- The most accurate method of prediction is to simulate the equivalent load



- We must understand the response of the probe circuit
- Sometimes we want a quicker method to estimate the probe affect

The Simplified Electrical Model of the Probe

- The probe's goal is to have a HIGH impedance



- However, there will always be:

  - series Inductance
  - parallel capacitance
  - parallel resistance

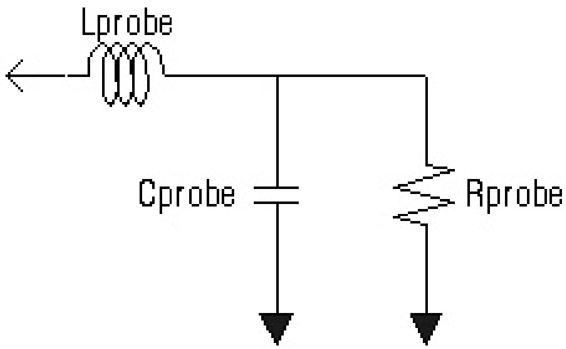
Lumped Capacitance Model

- If we assume that:

  the series inductance is small

  and

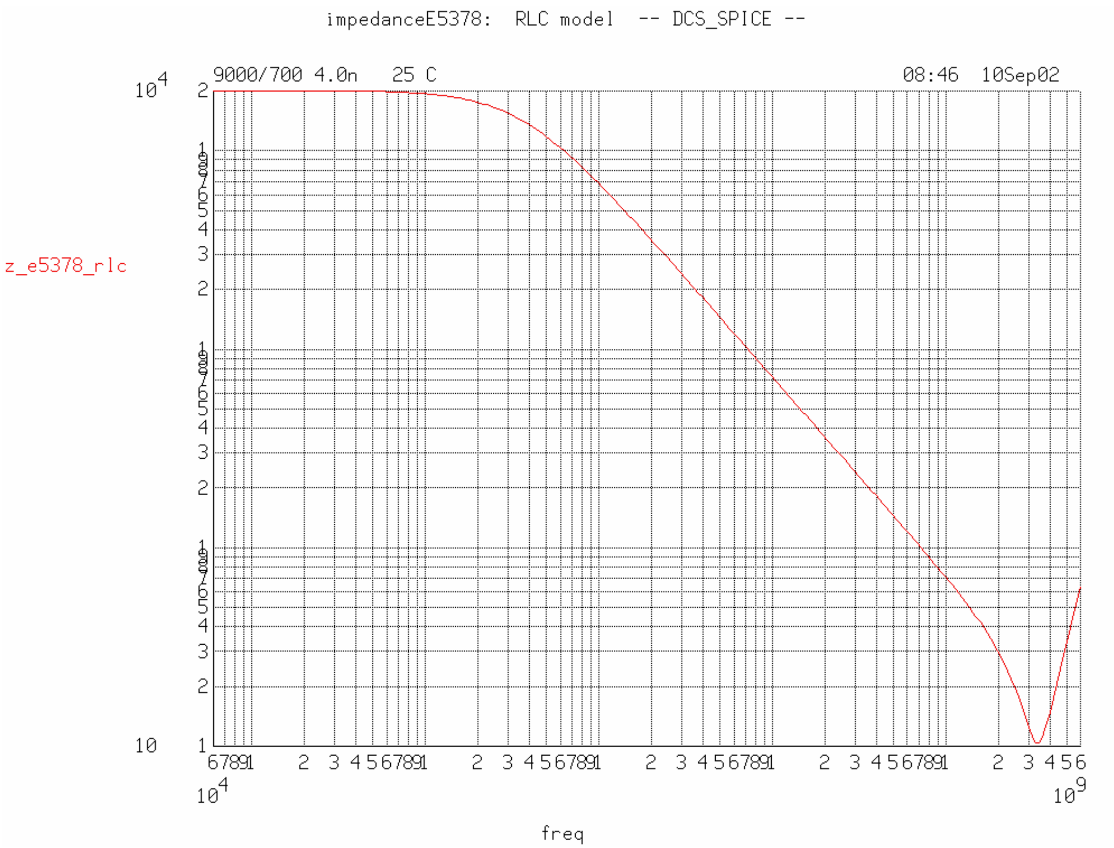
  the parallel resistance is high



- **The probe can be estimated as a lumped capacitance**
- **This is useful for quick hand calculations**
- **This is NOT as accurate as simulation**

Impedance Profile

Another method of prediction is to view the probe's impedance profile



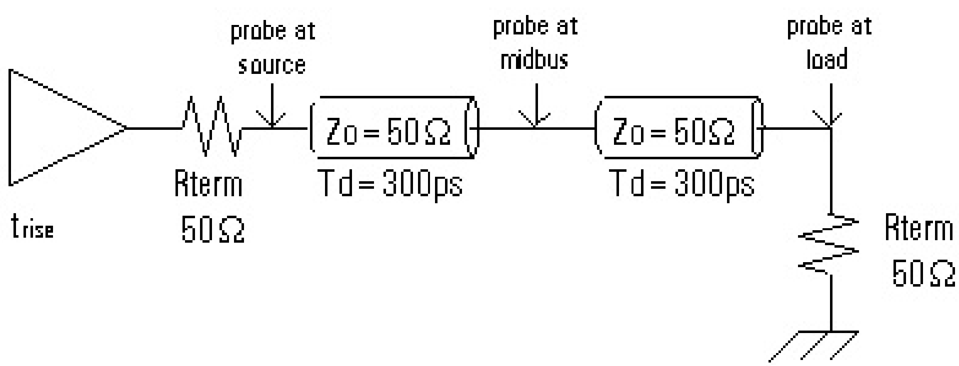
NOTE:

- High Z at DC
- RC Roll-off
- Resonance
- Inductive Nature

Probing Location

-The location of the probe affects:

- the target signal integrity AND
- the probe signal integrity

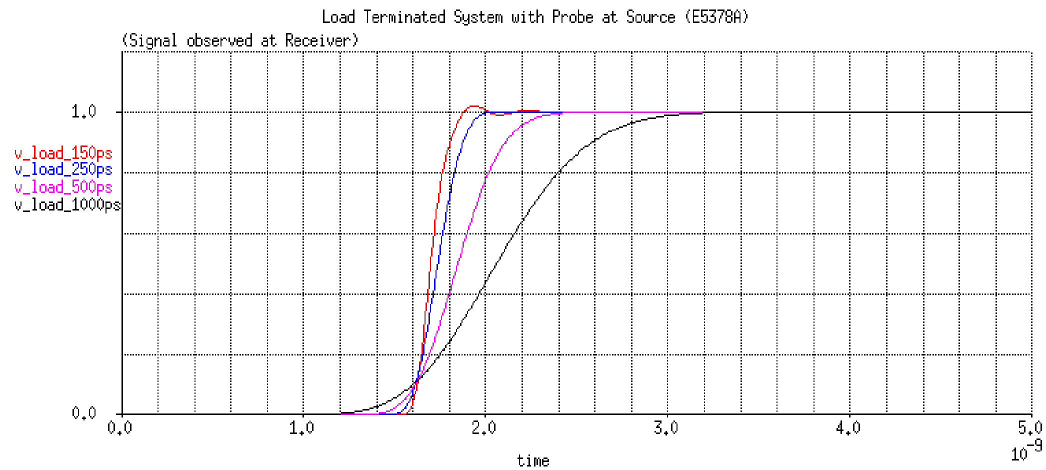


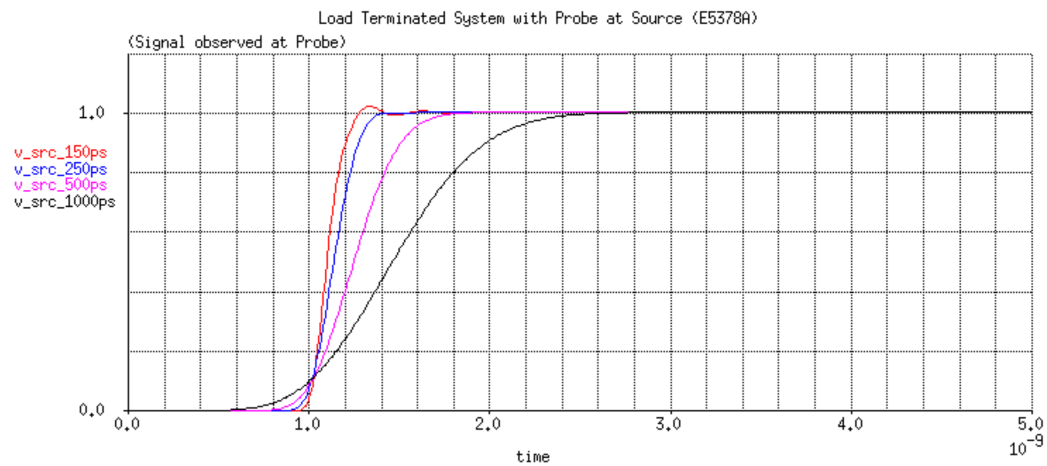
- The termination scheme and parasitics of the target affect the performance of the probe

- The location and loading of the probe affect the performance of the target

Probing Location Example #1

- Load Terminated System
- Probing at Source



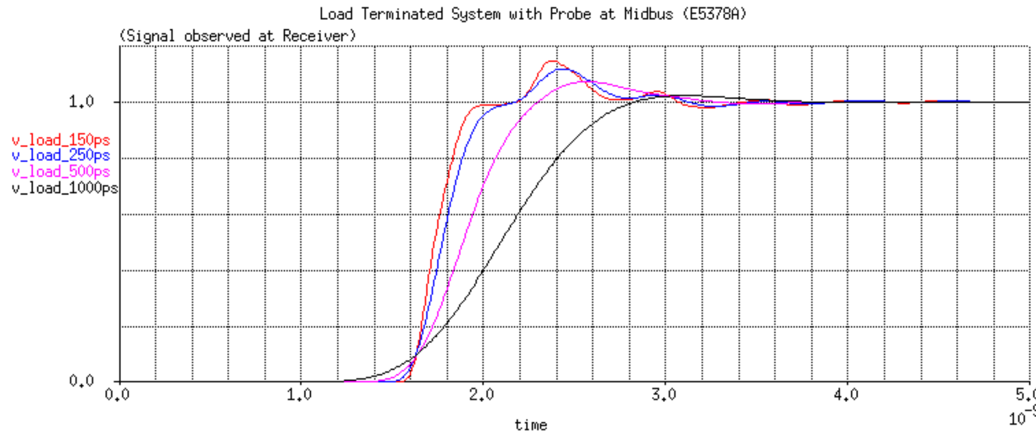


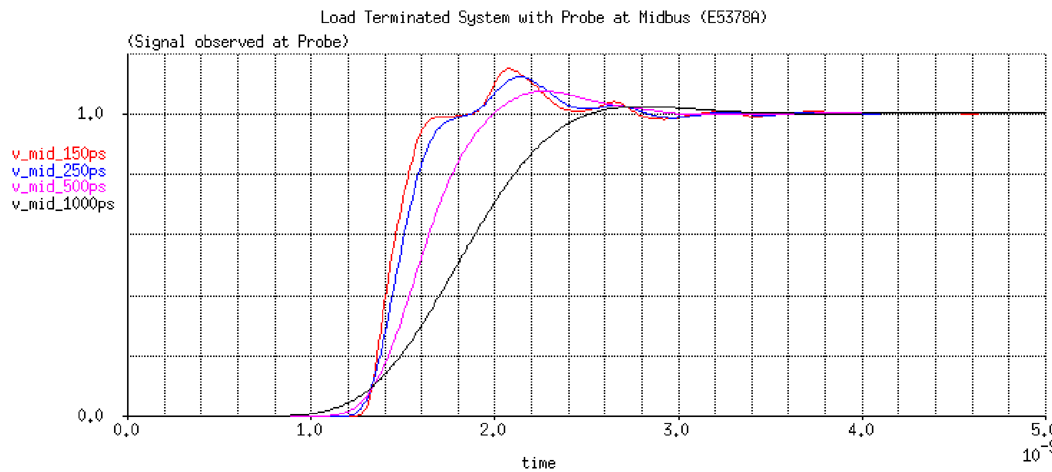
- 4 risetimes are shown (150ps, 250ps, 500ps, and 1000ps)
- Higher risetimes have higher frequency components which will see the “undesirable” regions of the probes response
- The response is good for both the target and the probe

Probing Location Example #2

- Load Terminated System
- Probing at Midbus

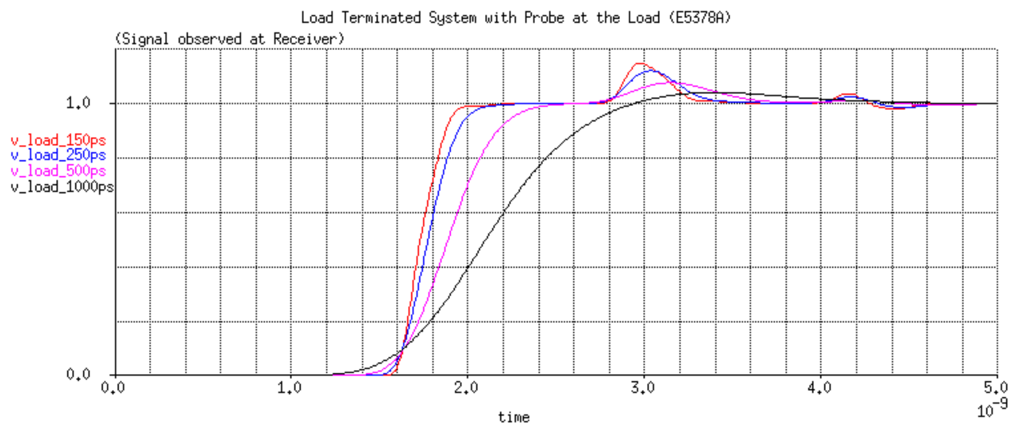
- The positive reflection present is due to the reflection of the discontinuity and its re-reflection off of the source.

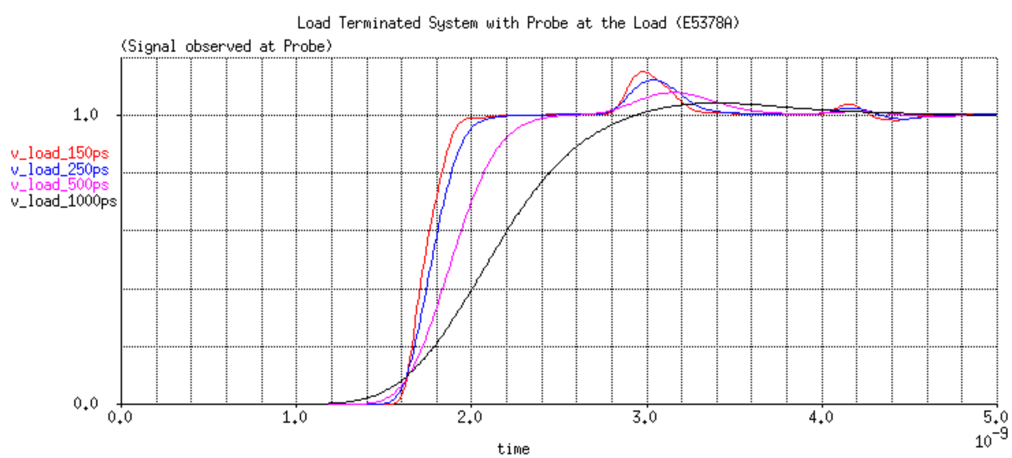




Probing Location Example #3

- Load Terminated System
- Probing at Load





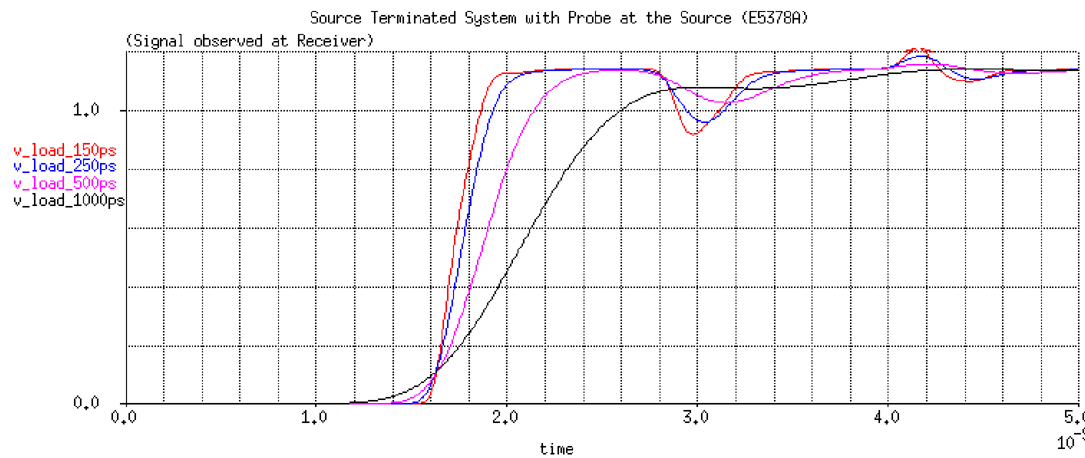
- Again, The positive reflection present is due to the reflection of the discontinuity and its re-reflection off of the source.

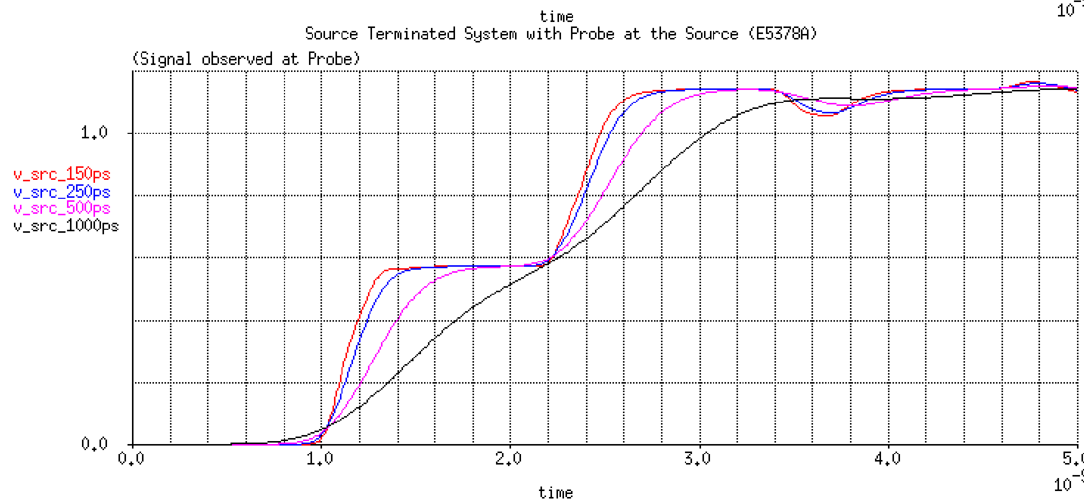
- Although in this case, it is further out in time.

Probing Location Example #4

- Source Terminated System
- Probing at Source

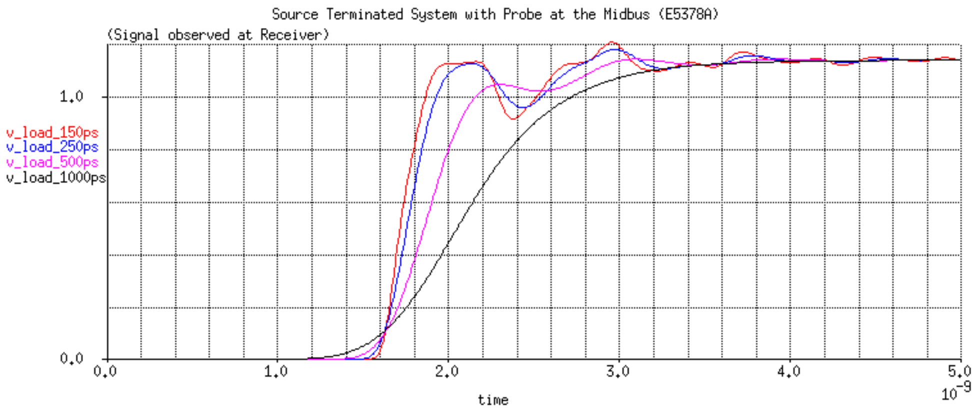
- The response at the receiver looks acceptable.
- However, the response at the probe tip is unacceptable.
- The flat region will be an “undetermined” logic level by the logic analyzer.

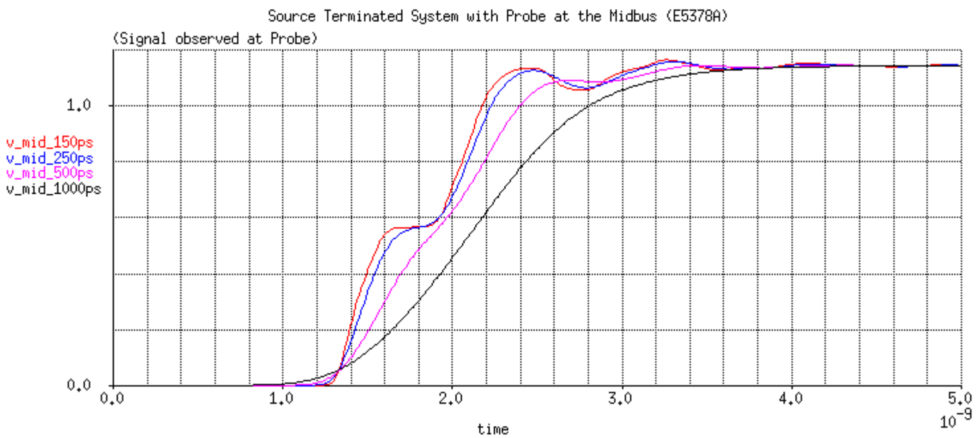




Probing Location Example #5

- Source Terminated System
- Probing at Midbus



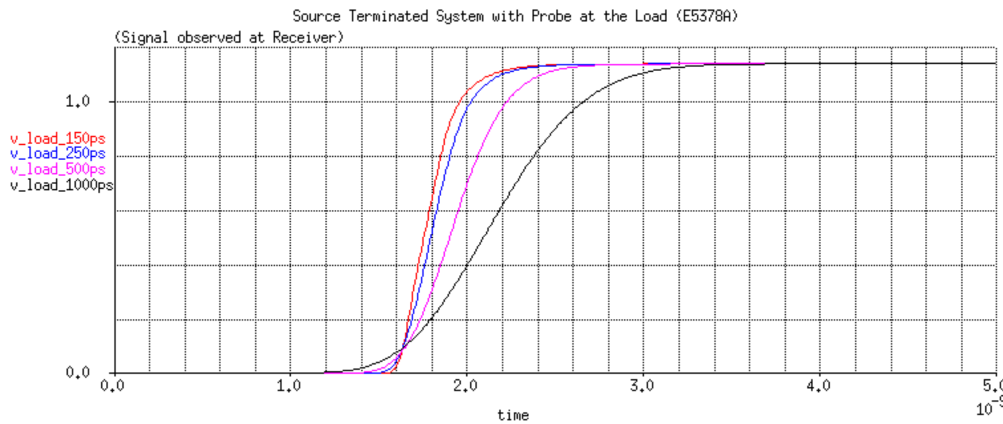


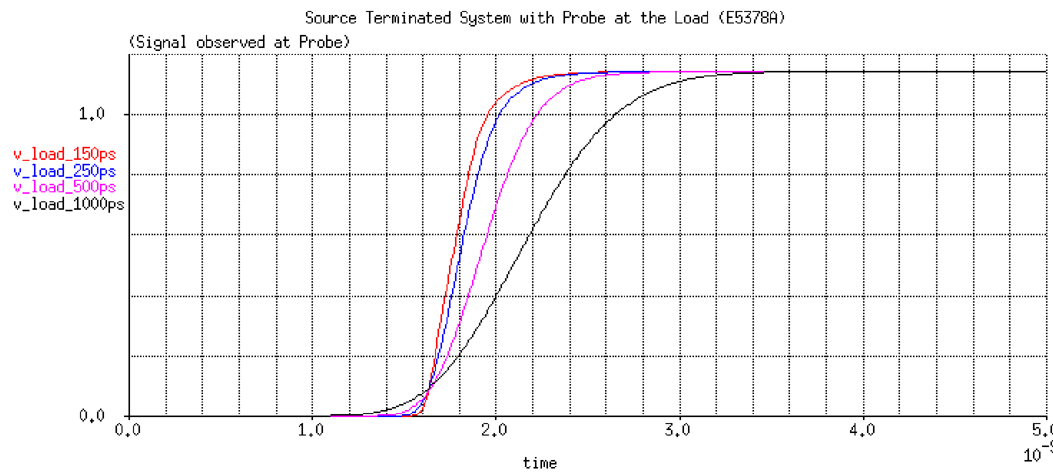
- Again, the flat region is present in the signal that the probe tip sees. This is unacceptable for the logic analyzer.

Probing Location Example #6

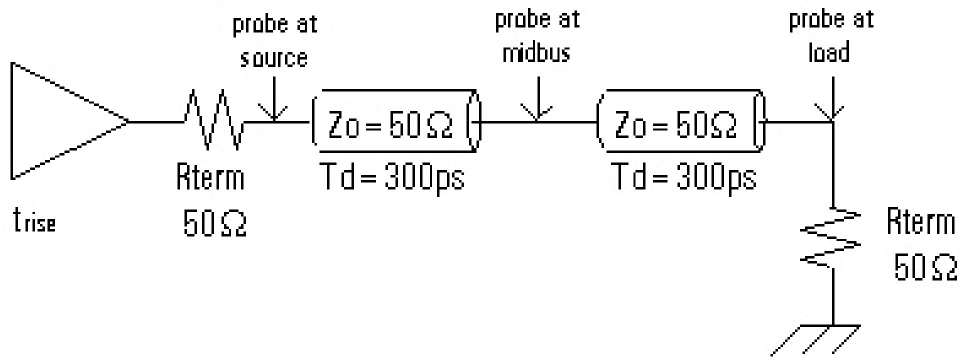
- Source Terminated System
- Probing at Load

- The response looks good at both the receiver and the probe tip.
- This is the optimal place to probe a source terminated system.





Probing Location Summary



1) **For a Load-Terminated System – place probe at the Source**
2) **For a Source-Terminated System – place probe at the Load**
3) **For a Double-Terminated System – place probe at Midbus**

The reason for placing the probe at the midbus is to reduce its effective time constant. Placing the load in the middle of the transmission line will give an effective R of Zo//Zo (usually 25Ω's)

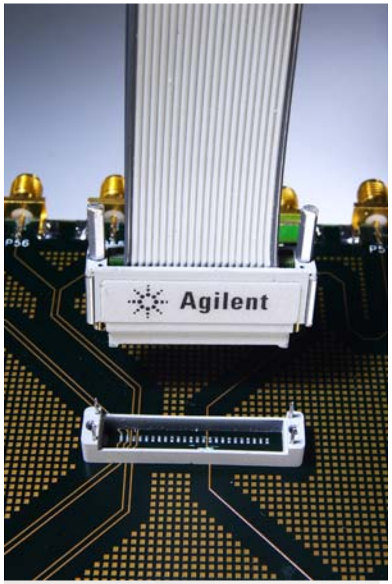
Probing Comparison

- The evolution of Logic Analyzer Probes has given the user the following:

  1) Lower Capacitive Loading
  2) Higher Resonant Frequency of the Probe Load
  3) Higher Bandwidth Probes
  4) Denser Connections

Probing Comparison

- The following examples show a comparison between 4 popular logic analyzer probes:



E5387A
Soft-Touch
(Cload = 0.7pF)

E5381A
Flying Lead
(Cload = 0.9pF)

E5378A
Samtec
(Cload = 1.5pF)

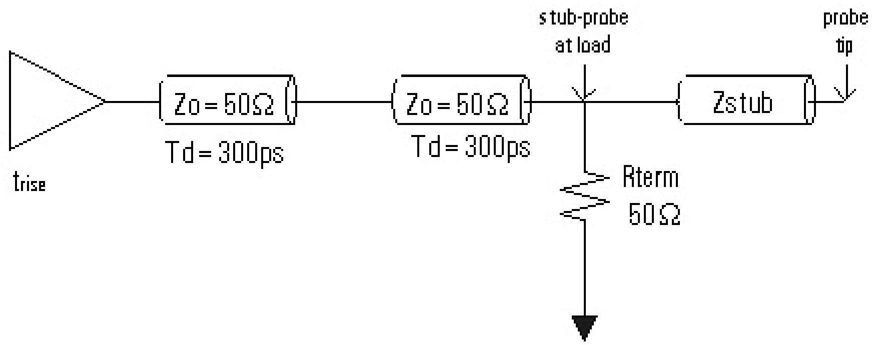
E5380A
Mictor
(Cload = 3.0pF)

Specific Probing Techniques

- Until now, we have assumed that the probe tip is directly connected to the target system without any distance between the two.

- In reality, the probe tip will have a finite distance between the target transmission line and the probe.

- The question then becomes, “How far away from the target can the probe tip be?”



Specific Probing Techniques (Stub-Probing)

- When there is a stub between the probe tip and the target, this is referred to as "Stub-Probing"

- The general rule is "No-Stubs"

- Any stub will add capacitive loading to the target and roll-off the signal that the analyzer sees.

Ex) The E5387A Probe (Cload=0.7pF) is located 1" away from the target connected through a 50 ohm microstrip line (C=3pF/in).

The total capacitive load of the probe is now 3.7pF.
The capacitance of the stub has dominated the loading of the probe.

Even 1" is a lot!

Specific Probing Techniques (Stub-Probing)

- The rule of thumb is to keep the electrical length of the stub less than 20% of the target's risetime.

- This allows the stub to be treated as a lumped capacitance and its adverse affects on the system can be easily predicted.

- If the stub is longer than this, the stub becomes a transmission line and reflections must be considered. This is BAD

Specific Probing Techniques (Stub-Probing Example)

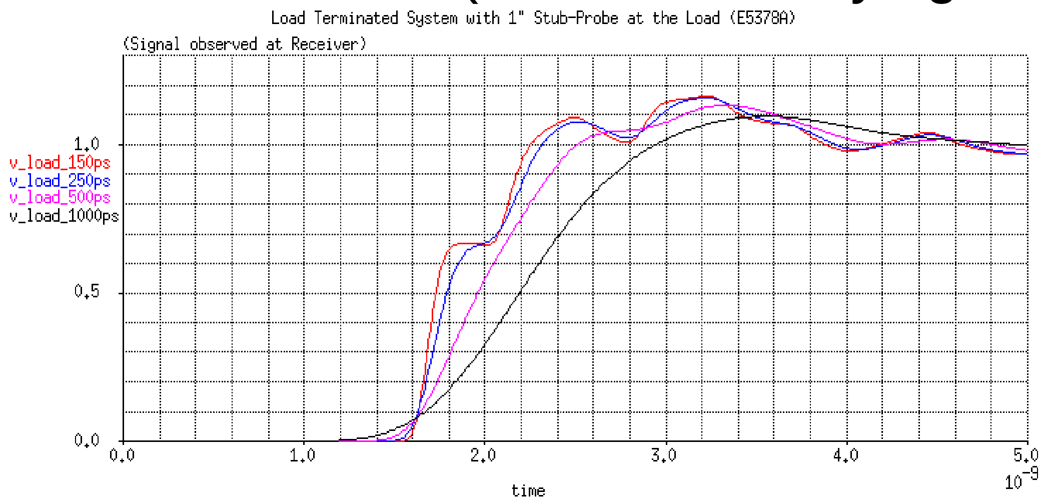
Given a system with:
- load terminated system
- propagation delay = 150ps/in
- trace capacitance = 3pF/in
- 1” stub between probe and load

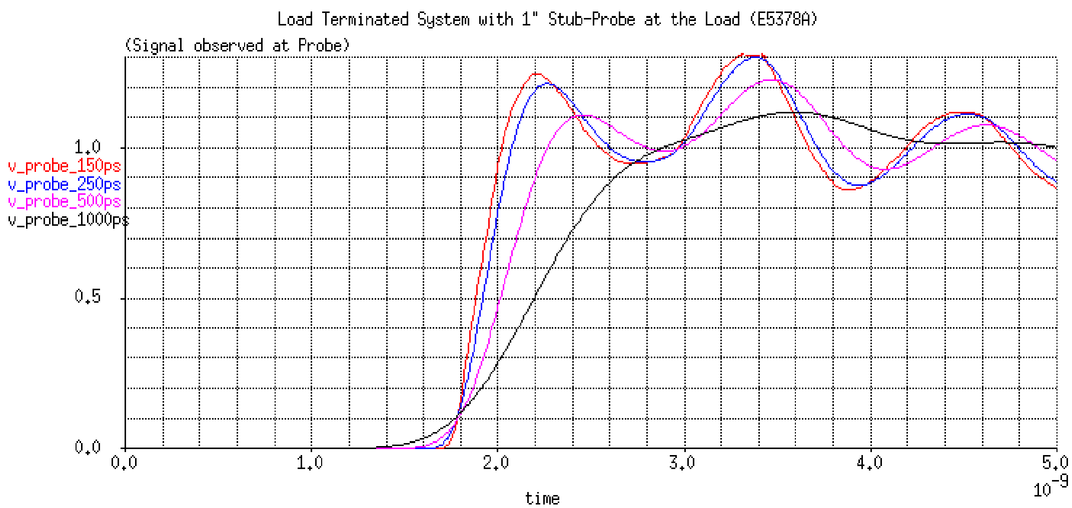
Risetime	Max-Electrical-Length	Max-Physical-Length	Capacitance
150ps	150ps*0.2 = 30ps	(30ps)/(150ps/in) = 0.2”	(.2”)*(3pF) = 0.6pF
250ps	250ps*0.2 = 50ps	(50ps)/(150ps/in) = 0.33”	(.33”)*(3pF) = 1.0pF
500ps	500ps*0.2 = 100ps	(100ps)/(150ps/in) = 0.67”	(.37”)*(3pF) = 2.0pF
1000ps	1000ps*0.2 = 200ps	(200ps)/(150ps/in) = 1.33”	(1.33”)*(3pF)= 4.0pF

- Only for the 1000ps risetime can we treat the 1” stub as a lumped capacitance.

- The 150ps, 250ps, and 500ps risetimes will see a distributed load and have reflections.

Specific Probing Techniques
(1" Stub w/ Varying Risetime)





- The 1000ps risetime is rolled off but does not have reflections.

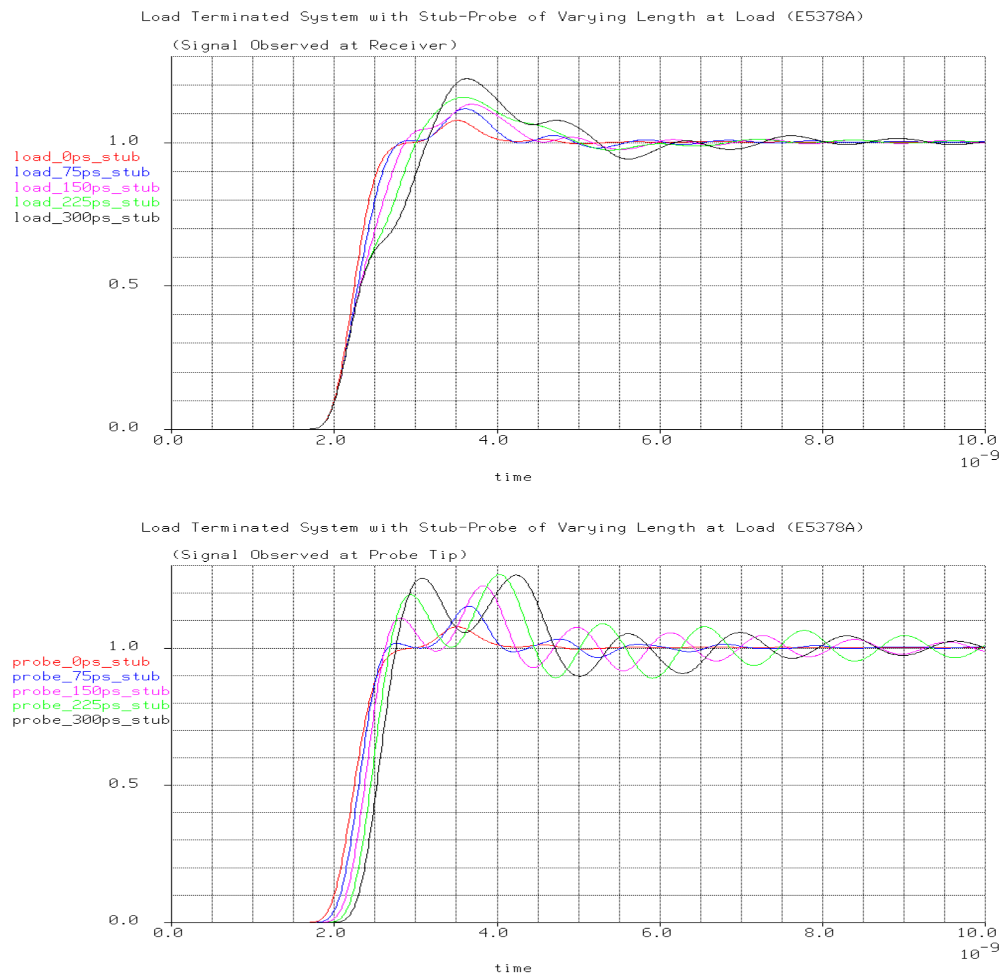
- The faster risetimes are seeing considerable ringing due to reflections off of the stub-probe.

- Summary: The faster the risetime, the shorter the stub that can be tolerated.

Specific Probing Techniques
(500ps Risetime w/ Varying Stub Length)

- **The stub length is varied from 0” to 2”.**

- **Notice that there are reflections still being observed at the probe tip up to 8ns after the initial edge.**

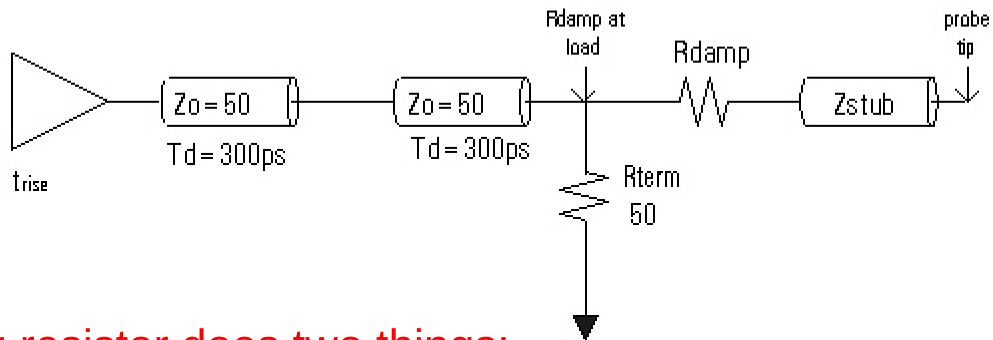


Specific Probing Techniques
(Damped Resistor Probing)

- If a stub cannot be avoided, a method called “Damped Resistor Probing” can be used.

- In this method, a resistor is placed at the target. This feeds a length of trace connecting to the probe tip.

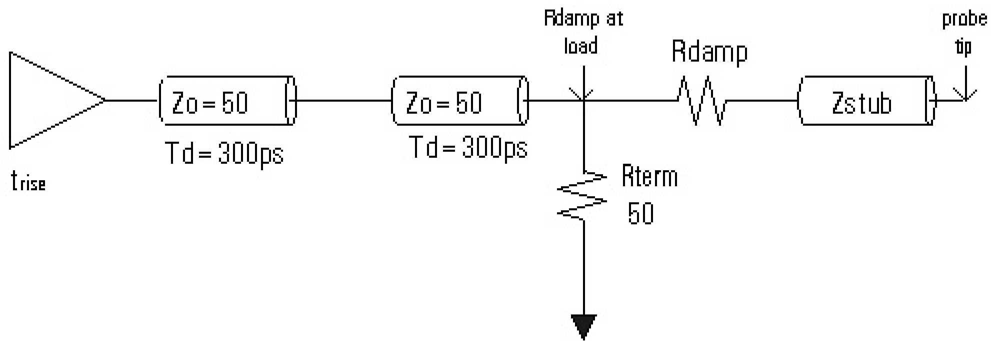
- This allows a longer length of trace to be used to connect to the probe tip.



The Damping resistor does two things:

1) It isolates the target from the trace capacitance
2) It dissipates the reflection energy contained on the stub

Specific Probing Techniques (Damped Resistor Probing)



Damped Resistor Consideration:

1) The damping resistor and the trace capacitance will form an RC filter that will roll off the signal that the analyzer sees.

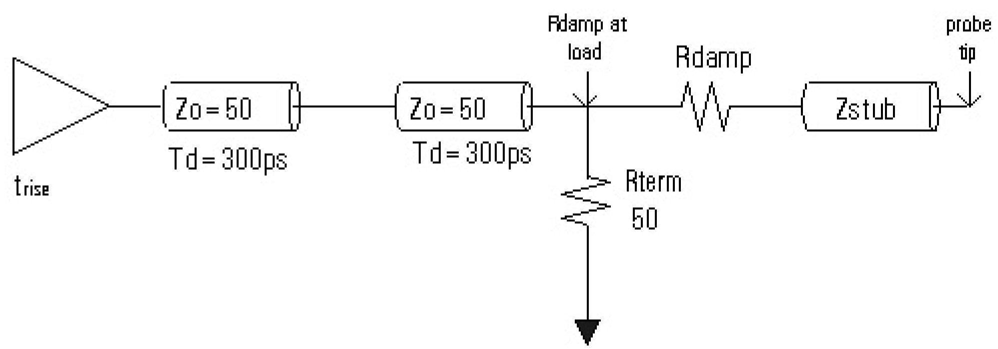
2) The maximum length of the trace will be dictated by the bandwidth needed at the probe tip.

Specific Probing Techniques (Damped Resistor Probing)

Damped Resistor Design Rules:

1) Choose a damping resistor that is 2.5x the impedance of the target.

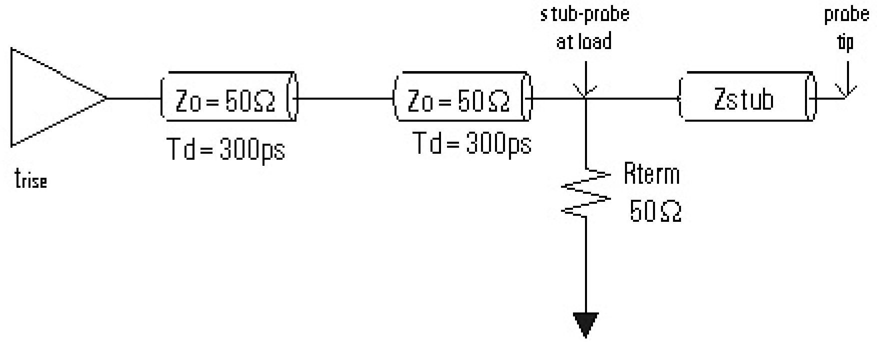
2) Keep the stub trace impedance as high as possible. This will reduce the capacitance per inch of the trace.



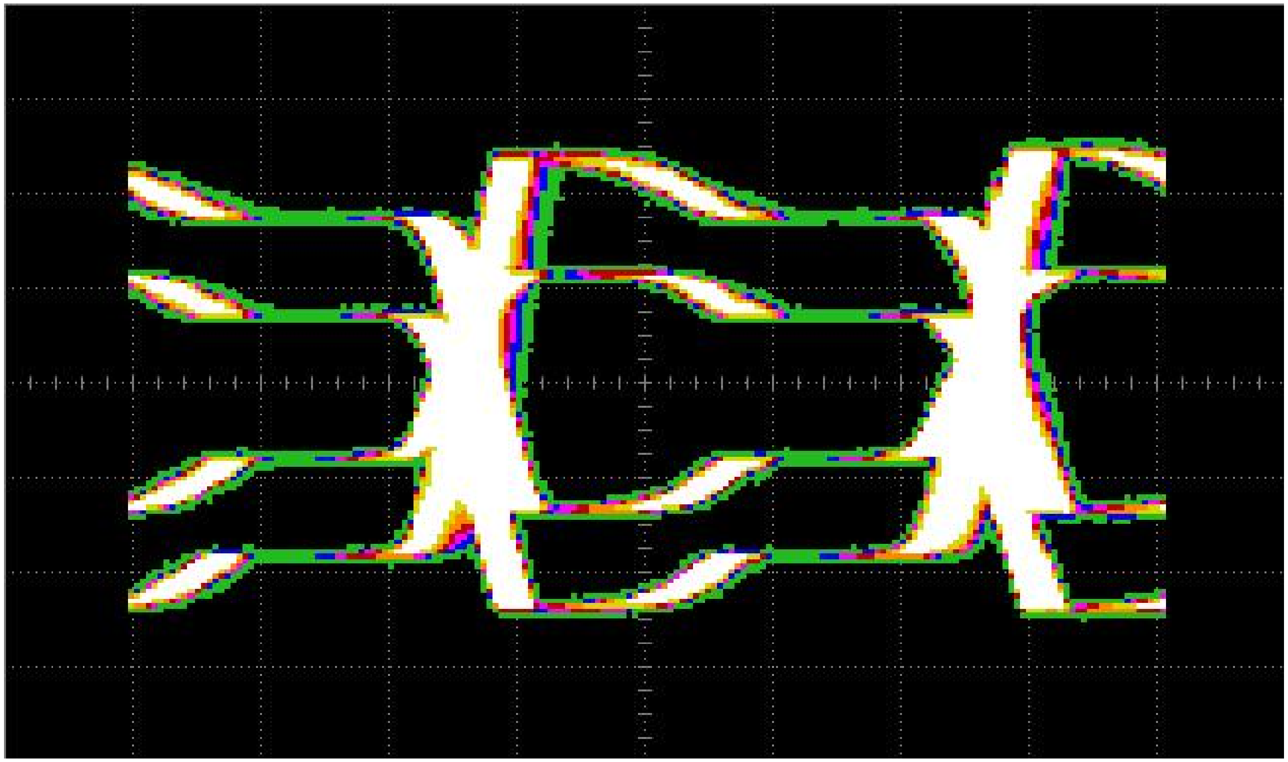
Specific Probing Techniques
(Eye Scan Example)

Eye Scan is a Signal Integrity Tool that maps the Eye Diagram of the Probed Signal

1) The E5387A Connector-less Probe is probing a load terminated system at the load through a 0.5” stub.

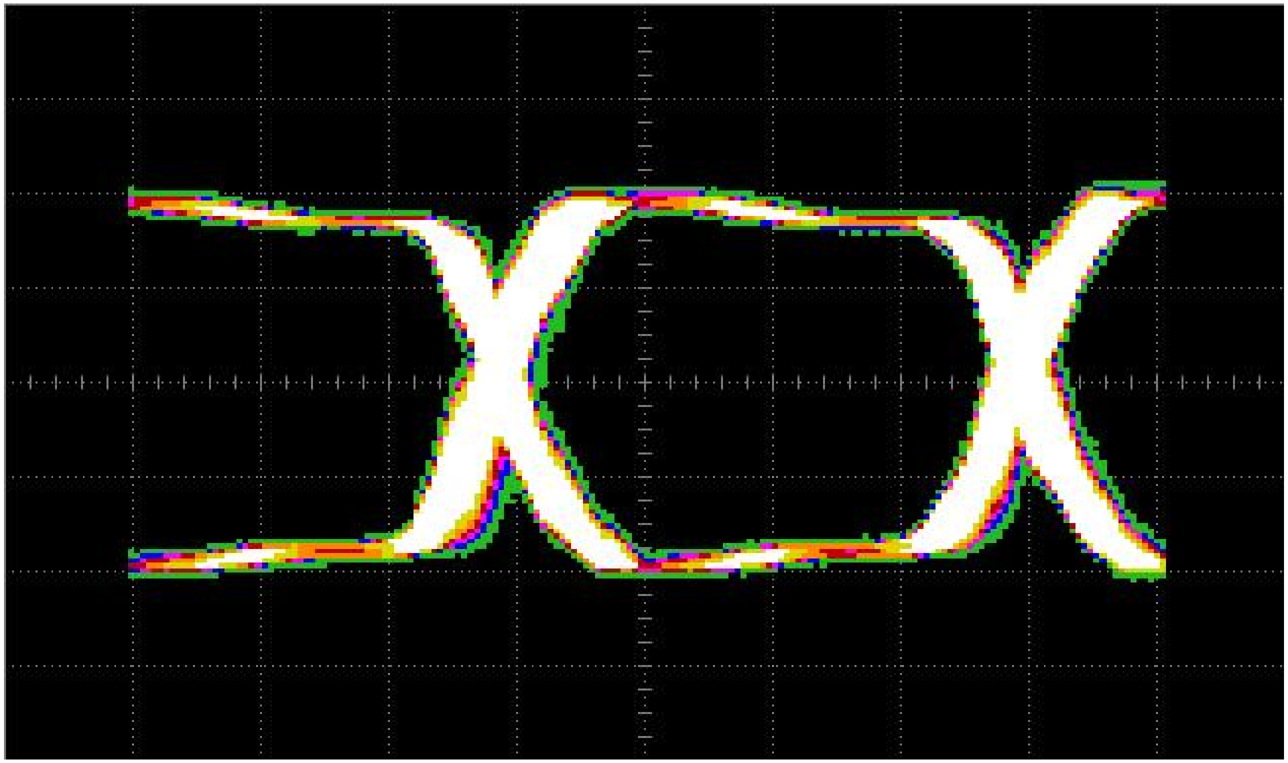


Specific Probing Techniques (Eye Diagram through 0.5" of Stub)



(500 Mb/s, 400mVpp)

Specific Probing Techniques
(Eye Diagram through with 125 Ω Damping Resistor)



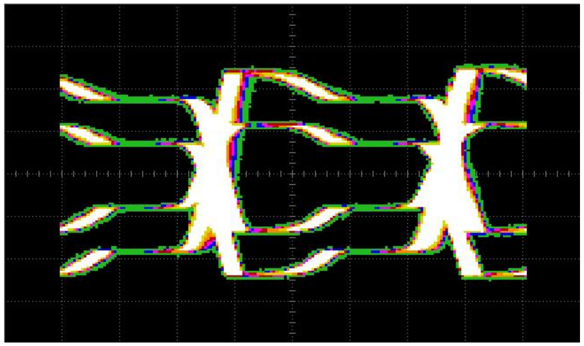
(500 Mb/s, 400mVpp)

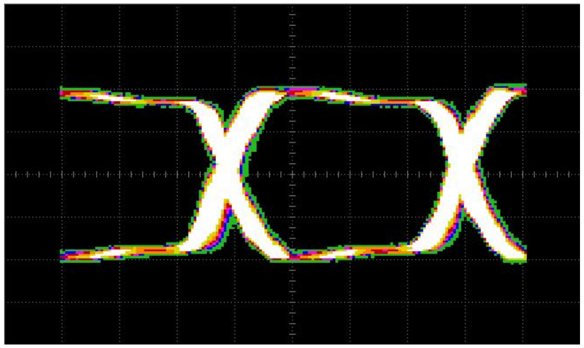
Specific Probing Techniques
(Damping Resistor Summary)

- Without Damping Resistor, the observed signal is distorted.

- With the Damping Resistor, the observed signal is a true analog representation of the target.

- With good probing, the signal integrity of the system can now be evaluated





Electrical Performance Summary

1) Methods for predicting the affect of the probe on the target:
- lumped capacitance hand-calculations
- impedance profile extraction
- simulation of equivalent load model (BEST)

2) Variables that affect the performance of the system and probe:
- probe load
- probe location
- target topology and margins

3) Specific probing Techniques:
- place probe tip directly on the target (BEST)
- stub-probing
- damped-wire probing

Modern Probing Solutions

Modern Logic Analyzer Probes fall into one of the four categories:

1) Connector-Based

2) Connector-Less

3) Flying Lead

4) Custom

Modern Probing Solutions

“Connector-Based”

- The user puts down a pre-defined connected on the target system.
- Signals are routed to the connector
- A logic analyzer probe with the opposite sex connector is plugged in

Advantages:

1) Easy to connect to target

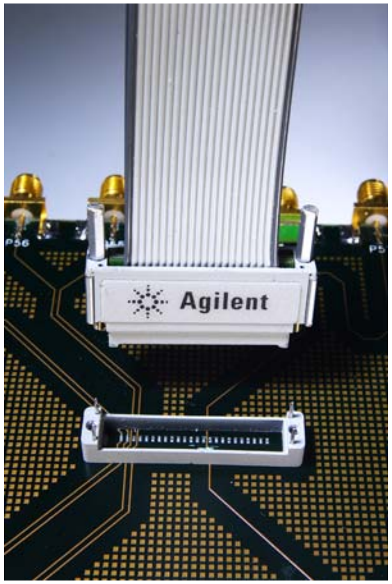
2) Robust Connection

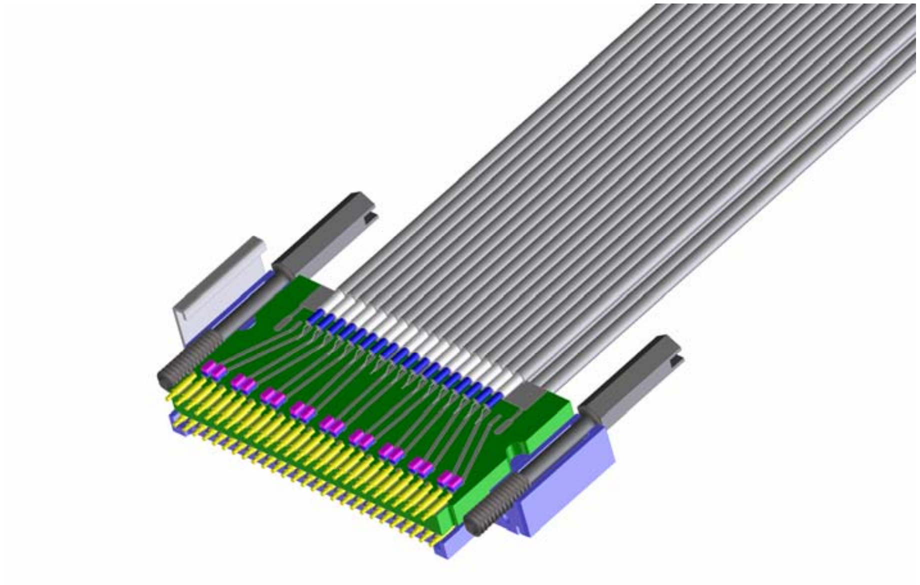
Modern Probing Solutions

“Connector-Less”

NEW!

- The user puts down a ‘landing pattern’ on the target system.
- The connector-less probe is then attached to the system with a ‘retention module’



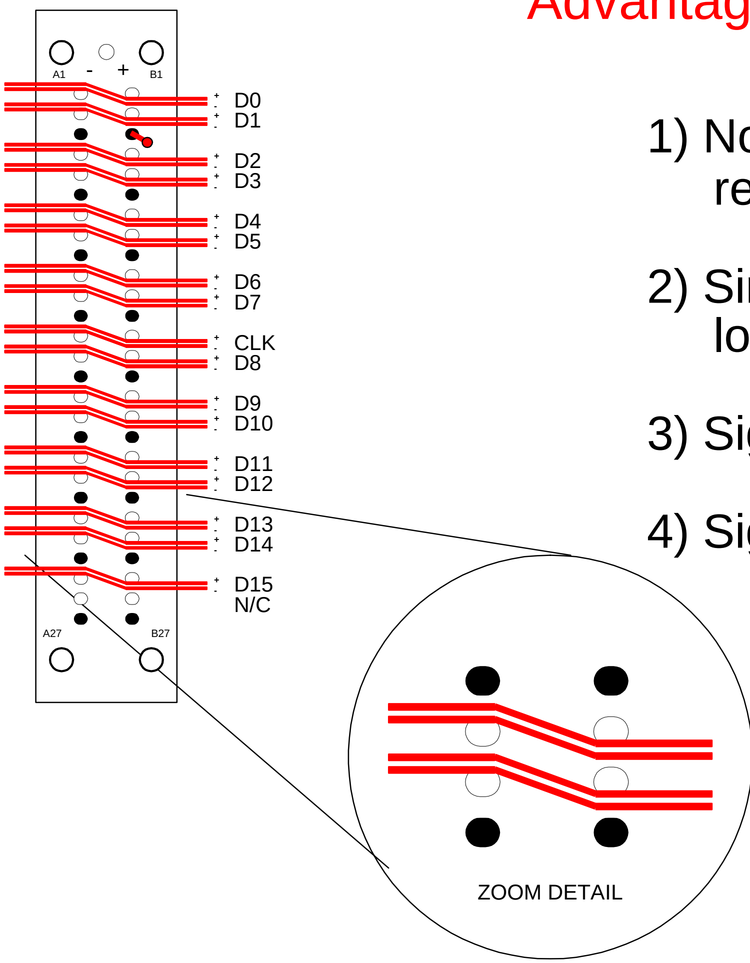


Modern Probing Solutions

"Connector-Less"

NEW!

Advantages:



1) No connector is needed so cost is reduced on the target.

2) Since the signal doesn't go through a connector, loading is reduced. (~0.7pF)

3) Signal routing is improved.

4) Signal Density is increased

Perfectly Suited for Embedded Memory Systems!

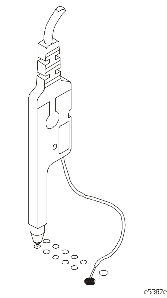
Modern Probing Solutions
“Flying Lead”

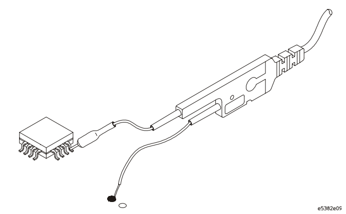
Advantages:

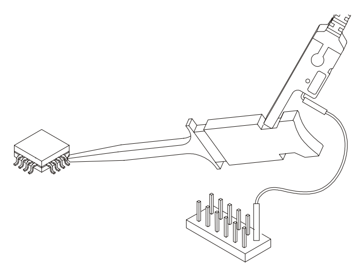
1) Signals that are not routed
to a connector can be probed.

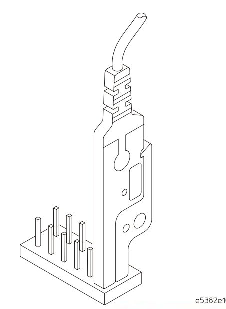
2) Accessories make most
connections possible.

3) Full Bandwidth





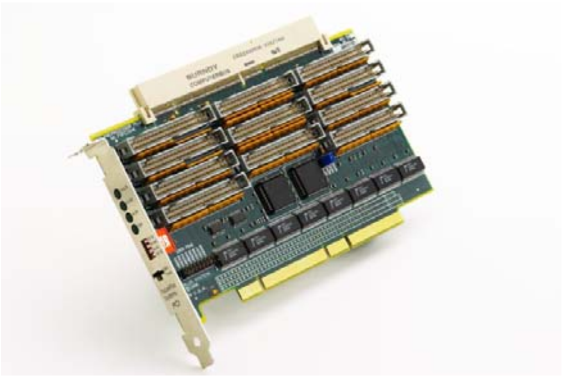


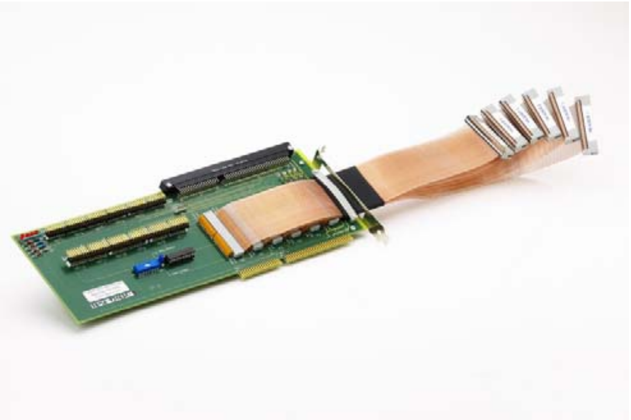


Modern Probing Solutions
"Custom"

- Designed specifically for an application or form factor

Ex) processors, microcontroller, memories, etc…

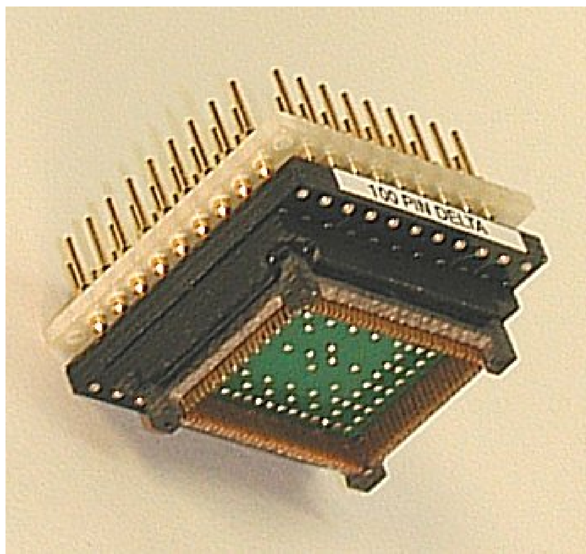




Modern Probing Solutions
“Memory System Specific”

- Custom Memory System Probes are Available

1) The probing connection has already been designed
2) The Logic Analyzer Vendor has considered the loading



“Chip Probe Adapter”
FS1107
by
FuturePlus Systems

Modern Probing Solutions
"DDR266"

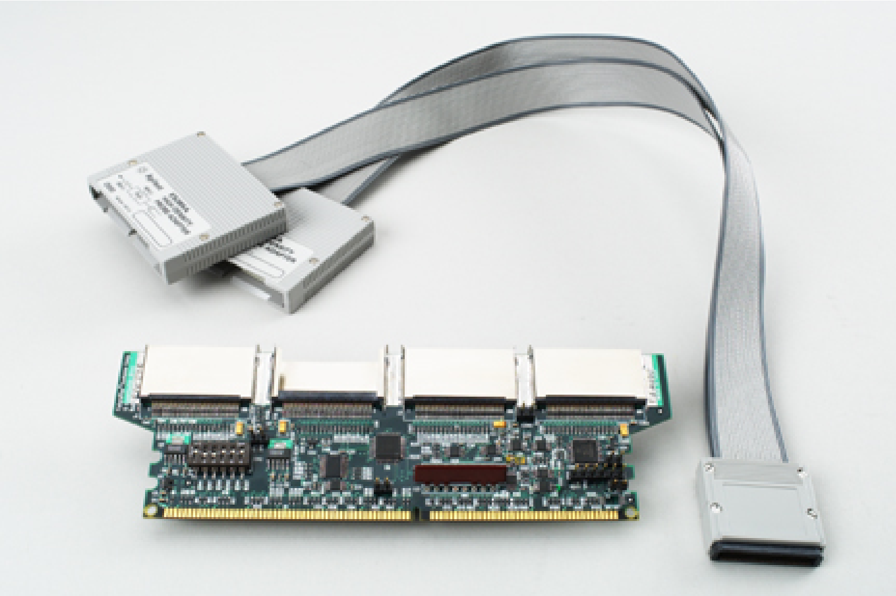
- Socketed Probing Solution for DDR266

"DDR266 Probe"
FS2330
by
FuturePlus Systems

Modern Probing Solutions

“DDR333”

- Socketed Probing Solution for DDR333



“DDR333 Probe”

FS2331

by

FuturePlus Systems

Summary

1) Electrical Affects of the target and the probe must be considered.

2) Mechanical Constraints of the probe must be considered.

3) Both electrical and mechanical affects contribute to the probes usefulness.

4) Many probing techniques are available to ensure successful probing of a high-speed digital system.

5) A variety of probe form-factors are available to best meet the need of industry.

Questions?