Broadband Impedance Matching for Inductive Interconnect in VLSI Packages

Brock LaMeres* Sunil P Khatri†
* Department of ECE, University of Colorado, Boulder, CO 80309.
† Department of EE, Texas A&M University, College Station TX 77843.

Abstract— **Noise induced by impedance discontinuities from VLSI packaging is one of the leading challenges facing system level designers in the next decade. The performance of IC cores far exceeds that of current packaging technology. The risetimes of IC signals require that the interconnect of the package be treated as transmission lines. As a result, impedance discontinuities in the package cause reflections which may result in intermittent switching of digital signals and edge time degradation, both of which limit system performance. The major cause of the impedance discontinuity in the package is the high inductance of the wire bond interconnect. To compensate for this problem, capacitance can be placed near the wire bond to reduce its effective impedance over a given frequency range. This paper presents the application of this impedance matching technique for use in broadband digital signals that are prevalent in modern VLSI designs. Both static and dynamic compensation approaches are presented. The static compensator places pre-defined capacitances on the package and on the IC to surround the wire bond inductance. The dynamic compensator places a switchable capacitance on the IC that can be programmed to a desired value, thereby enabling the designer to overcome design and manufacturing variations in the wire bond. Both techniques presented are shown to bound the reflections of the wire bond to less than 5% (down from 20% for an uncompensated structure) for wire bonds up to 5mm in length, and for frequencies up to 3GHz. In addition, both circuits utilizes less area than a typical wire bond pad, making them ideal for placement directly beneath the wire bond pads.**

I. Introduction

Wire bonding is the most commonly used packaging methodology to connect signals from a silicon die to corresponding pads on a package substrate. Wire bonding is a fast and inexpensive process, which explains its popularity. While this technology has been refined over the years to provide a robust and inexpensive mechanical connection, the electrical parasitics associated with wire bonding are becoming a serious problem at today's data rates. Wire bonds tend to be highly inductive due to their large current return loops and distance from other conductors. As a consequence, wire bonds tend to have a higher impedance than the traditional 50Ω traces used for packages and for printed wiring boards (PWB's). The following expression gives the characteristic impedance of a loss-less transmission line and is used to model the impedance of the wire bond structure. Here, L and C are the inductance and capacitance per unit length of the transmission line.

$$Z_0 = \sqrt{\frac{L}{C}} \tag{1}$$

The wire bond is the largest source of excess inductance in the package [1], resulting in a large Z_0 and thus causing unwanted signal reflections. Reflections on the transmission line are dictated by the reflection coefficient $\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}$

The magnitude of the reflected signal is given by:

$$V_{reflected} = V_{incident} \cdot \Gamma \tag{2}$$

Similarly, the magnitude of the transmitted signal is given by $V_{transmitted} = V_{incident} \cdot (1 - \Gamma)$.

These equations illustrate that any impedance mismatch due to a wire bond will result in reflected energy in addition to limiting the energy transmitted to the receiver.

As data rates of digital systems continue to increase, the speed limitations caused by reflections due to wire bonds are becoming a dominant factor in system performance. Aggressive package design such as flip-chip bumping can reduce the inductance present in the Level 1 (IC to Package) interconnect [1]. However, these techniques are costly and do not have the flexibility and simplicity of a wire bond process. Any technique that can increase the throughput of a wire bond package will greatly assist in keeping the packaging cost down as speeds increase.

In this paper, we present two techniques to reduce the impedance of the wire bond interconnect by adding capacitance near the structure. The first technique is a static approach, in which capacitance is added to the package and on the IC near the wire bond pads. In order to prevent increased cost, embedded capacitors (EC) are used in the package substrate based on standard printed wiring board (PWB) processes. Embedded package capacitors are ideally suited to be implemented directly beneath the wedge bond pads on the package substrate [2], [3]. Two types of on-chip capacitors were evaluated for performance and area efficiency. The first is a Metal-Insulator-Metal (MIM) capacitor which is implemented in the upper metal layers of the IC. The MIM capacitor has the advantage that its value is independent of bias voltage [4]. However, it requires a larger relative area compared to other on-chip capacitor techniques. The second type of on-chip capacitor that was evaluated was a device-based structure. This type of capacitor uses the MOS device polysilicon gate capacitance. This type of capacitor has a much higher capacitance density over the MIM capacitor, but suffers from bias voltage variation [5].

The second impedance matching technique is a dynamic compensator. In the dynamic compensator, a programmable circuit is implemented on-chip that will switch in different values of capacitance to the wire bond pad. The circuit consists of CMOS pass gates that selectively connect different values of on-chip capacitance to the wire bond pad. The diffusion capacitance of the pass gates are considered in the calculation of the total excess capacitance that is switched in to compensate for the wire bond inductance. The circuit is designed to have enough compensation range to cover reasonable lengths of wire bonds [1]. In addition, the programmability of the capacitance negates any process variation since the capacitance can be "dialed in" after IC fabrication and packaging. As with the static compensator, two types of on-chip capacitance were evaluated for performance and area (MIM and Device-based).

We demonstrate that both techniques can successfully compensate for wire bond lengths up to 5mm using either the MIM or Device-based capacitors. Experimental results show that for rise times up to 117ps (equivalent to 3GHz using the risetime-bandwidth product rule [6]), the compensators can bound the impedance discontinuity to <5%. This compares to discontinuities of up to 20% for uncompensated 5mm bond wires. In addition, the impedance of the compensated structure can be held to within 10Ω of the design target (typically 50Ω) up to a much higher frequency. For a 3mm wire bond length, whose impedance strays to +/- 10Ω from the 50Ω target at 3.1GHz, our approaches can hold the impedance to within 10Ω of the target up to 4.8GHz using a static compensator and up to 6.8 GHz using a dynamic compensator.

The rest of this paper is organized as follows. Section II presents previous work in the area of capacitor implementations that are used in our compensators. Section III describes the methodology used to achieve the impedance match. Section IV presents the electric extraction results for the package geometries studied i

Proceedings of the 2005 International Conference on Computer Design (ICCD'05)
0-7695-2451-6/05 $20.00 © 2005 IEEE

Sections V and VI describe the design of the static and dynamic compensators respectively. Experimental results are given in Section VII and conclusions drawn in Section VIII

II. Previous Work

A. PWB Embedded Capacitors

Work done in [7] and [8] showed an implementation of an embedded film capacitor (EFC) using standard copper clad lamination. A standard dielectric material was used (FR-4) with a dielectric constant 4.6. The capacitor's effectiveness was compared to that of 16 discrete capacitors in the application of power/ground plane impedance reduction. It was found that the ESL using the best EFC configuration was reduced to 106pH from 270pH when using 16x100nF discrete decoupling capacitors.

Additional improvement to embedded capacitors was illustrated in [2] for use in low-cost organic PWB's. In this case, polymer-ceramic nanocomposite materials were used to achieve high k (25-50) thin films. The photoimageable polymer-ceramic material has a low processing temperature ($< 200^oC$) which could be applied to a standard PWB process. The thickness of the EFC's was varied from $25um$ to $50um$. The authors reported a 20x reduction in simultaneous switching noise (SSN) over a traditional PWB.

A more advanced high k material was presented in [9]. This work presented a hydrothermal barium titanate thin film to create EFC's. This process is attractive due to its low temperature processing ($< 160^oC$) and ability to be integrated onto organic PWB's. The process achieved extremely high k values (> 350) with capacitance densities of $1uF/cm^2$. The EFC's reported a 30% reduction in SSN over a frequency range from 0.01MHz to 500MHz.

All of these approaches lay the foundation for a low-cost embedded PWB capacitor implementation using standard process technology.

B. On-Chip Embedded Capacitors

Metal-Insulator-Metal (MIM) capacitors were analyzed in [4] and [10] to study the effect of common on-chip insulator materials on the capacitance density. In [4], the authors demonstrated fabrication of MIM's using three different dielectric materials (Oxide, Nitride, and Oxynitride). Over an acceptable range of thicknesses, the dielectrics studied produced capacitance densities from $1.4fF/um^2$ to $2.8fF/um^2$. This work demonstrated the feasibility of implementing high-density on-chip capacitors using both $90nm$ and $0.13um$ CMOS process steps.

In [3] it was illustrated that active circuitry could be integrated directly beneath the wire-bond pads. It was demonstrated that ring-oscillator circuits in a $0.13um$ CMOS process suffered no noticeable degradation in gate delay or cycle time from being placed directly beneath the pads. Gate delays of the structures beneath the bond pads matched very closely with the delays measured at the center of the die. While this approach was not explicitly utilized for use in decoupling applications, the proximity of the resulting device gate capacitance to the inductance of the wire-bond makes it ideal for achieving a non-distributed decoupling or matching network. This technology lends itself well to implementing device capacitors directly beneath the wire-bond pads.

For this work, MIM-based and Device-based on-chip capacitors are used in the compensator designs. In each case, the capacitors are implemented directly beneath the wire bond pad to achieve the closest proximity to the wire bond inductance.

III. Methodology

In order to reduce the impedance of the wire bond structure, excess capacitance must be added near the wire bond. The excess capacitance (C_{comp}) needed to match the wire bond structure to 50Ω can be derived from equation 1 and is given by:

$$C_{comp} = \frac{L_{wb}}{50^2} - C_{wb} \quad (3)$$

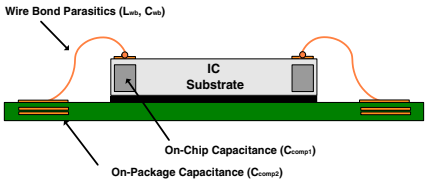

Fig. 1. Location of Compensation Capacitors and Wire Bond Parasitics

A. Compensator Proximity

If the compensation capacitance resides close to the wire bond, the resulting structure can be modeled as a lumped element for much higher frequencies. For this work, a 117ps rise time (equivalent to 3GHz using the risetime-bandwidth product rule [6]) is used to evaluate the compensators. This rise time is sufficient to model the majority of inter-chip busses present today [1].

Typically, a structure is considered a lumped element when its electrical length (i.e. its propagation delay) is less than 20% of the highest rise time in the system [11]. Using a 117ps risetime and a worst case dielectric constant of silicon nitrate (ϵ_r=7) to determine the electrical length of an integrated structure, the acceptable proximity of the compensation capacitance to the wire bond can be found. For this work it is found that the compensation capacitance must be within 2.6 mm of the wire bond [6] for it to be accurately modeled as a lumped impedance for a 117ps rise time. From the work cited in Section II, it is shown that capacitor elements can be implemented directly beneath the wire bond pads on the package and on-chip. This is the optimal electrical location for the capacitors in addition to being the least area intrusive.

The first compensation capacitor location is beneath the wire bond pad on-chip (C_{comp1}). This capacitance is implemented using either a MIM-based or Device-based component. The second location is beneath the wire bond pad on the package substrate (C_{comp2}). This capacitance is implemented using an embedded parallel plate structure. Figure 1 show the location of the compensation capacitors.

B. Static Compensation

In the static compensator methodology, pre-determined fixed capacitance is placed on-chip (C_{comp1}) and on-package (C_{comp2}). The capacitance values chosen are based on wire bond parasitics that result from the package design. The variation in wire bond process is also considered in the selection of the capacitor values. The static compensator has the advantage that capacitance can be placed on both sides of the wire bond inductance. This has the effect that the wire bond and compensation structures behave as a lumped element.

In the static compensator, the net compensation capacitance is given by:

$$C_{comp} = C_{comp1} + C_{comp2} \quad (4)$$

Using equation 1 to describe the impedance of the statically compensated structure, the impedance of the wire bond becomes:

$$Z_{0-static} = \sqrt{\frac{L_{wb}}{C_{wb} + C_{comp1} + C_{comp2}}} \quad (5)$$

C. Dynamic Compensation

In the dynamic compensator methodology, capacitance is only placed on-chip (C_{comp1}). This capacitance is programmable, allowing the compensator to successfully match impedance across variations in the wire bond inductance. The programmability means that the designer does not need to know the exact wire bond inductance prior to IC fabrication. This has the advantage that the dynamic compensator can accommodate process and design variations.

In the dynamic compensator, the net compensation c
given by:

$$C_{comp} = C_{comp1} \quad (6)$$

Using equation 1 to describe the impedance of the dynamically compensated structure, the impedance of the wire bond becomes:

$$Z_{0-dynamic} = \sqrt{\frac{L_{wb}}{C_{wb} + C_{comp1}}} \quad (7)$$

IV. Electrical Modeling

The first step in designing the compensation networks is to model the electrical parameters of the structure making up the package interconnect. For this purpose, we use a $5mm$ x $5mm$, wire-bonded silicon die that is mounted to a 22x22, $1mm$ pitch BGA package. The package uses a $1.27mm$ thick $GETEK^{©}$ substrate with traces designed to have a characteristic impedance of 50Ω using trace widths of $0.1mm$. The package is mounted to a $200mm$ x $250mm$ main PWB through standard controlled collapse solder ball technology. The main PWB uses a $1.575mm$ thick $GETEK^{©}$ substrate with traces designed to have a characteristic impedance of 50Ω using trace widths of $0.127mm$. The wire bonds and planes that form the embedded capacitors were modeled using the *Raphael* EM Field Solver [12]. Table I lists the electrical parameters for the structures modeled. For all structures, the worst case path is modeled.

A. Wire Bond Interconnect Modeling

The connection from the silicon die to the package substrate is formed using standard wire-bond technology. The wire bond is a gold wire with a diameter of $25um$. The connection to the die is made using a *ball bond* to a $100um$ x $100um$ aluminum pad. The connection to the package is made using a *wedge bond* to a $100um$ x $400um$ gold plated pad. The net length of the wire-bond was varied from $1mm$ to $5mm$.

B. On-Chip Capacitor Modeling

For this work, on-chip capacitors are implemented in two ways. The first type of on-chip capacitor is a Metal-Oxide-Metal (MIM) structure. In this work a MIM was implemented on layer 3. The MIM that was modeled had an area of $100um$ x $100um$ with $t_{ox} = 600A^{\circ}$ and $\epsilon_r = 7$ (Si_3N_4). The MIM achieved $1.15fF/um$ with constant capacitance versus applied voltage. This type of capacitor is suited well for impedance matching on signal paths where the bias voltage changes widely.

The second type of on-chip capacitor is a device-based structure. This capacitor is created by connecting the source and drain of a NMOS transistor to ground and using the gate as the positive terminal of the capacitor. This type of capacitor has a very high density due to the thin plate separation (t_{ox}). For the $0.1um$ process used in this work [13], [14], [15], $t_{ox} = 25\mathring{A}$ with $\epsilon_r = 3.9$ (SiO_2). The drawback of this type of capacitor is its variability with respect to the applied voltage. For the capacitor in this work, the value changed from $27pF$ to $138pF$ ($100um$ x $100um$) as the bias voltage changed from $V_G = 0v$ to $V_G = 1.5v$.

C. Package Capacitor Modeling

Within the package, the most cost effective design for the capacitor is an embedded structure. The embedded capacitor within the package substrate is implemented using standard parallel plate structures. Within the package, the minimum plane to plane separation allowed under normal process is $0.051mm$. A 50Ω stripline transmission line is designed using a lower dielectric separation of h_{below}=$0.051mm$ and a upper dielectric separation of h_{above}=$0.279mm$. This type of construction yields a signal impedance of 50Ω while also achieving the highest capacitance density allowed by process on the same layer. This construction yielded a capacitance density of $420fF/mm^2$.

V. Static Compensator Design

Using the electrical parameters from Table I and equations 4 and 5, the values of C_{comp1} and C_{comp2} for the static compensator can be found. Table II lists the optimal capacitor values to match the wire bond inductances (Table I) to 50Ω. Table III lists the corresponding sizes to implement the impedance matching capacitors.

$Length_{wb}$	C_{comp1}	C_{comp2}
1 mm	102fF	102fF
2 mm	208fF	208fF
3 mm	325fF	325fF
4 mm	450fF	450fF
5 mm	575fF	575fF

TABLE II
Static Compensation Capacitor Values

$Length_{wb}$	$C_{comp1-MIM}$	$C_{comp1-Device}$	$C_{comp2-EC}$
1 mm	10μm x 10μm	2.7μm x 2.7μm	388μm x 388μm
2 mm	14μm x 14μm	3.9μm x 3.9μm	554μm x 554μm
3 mm	18μm x 18μm	4.9μm x 4.9μm	692μm x 692μm
4 mm	21μm x 21μm	5.8μm x 5.8μm	815μm x 815μm
5 mm	24μm x 24μm	6.5μm x 6.5μm	921μm x 921μm

TABLE III
Static Compensation Capacitor Sizes

VI. Dynamic Compensator Design

A. Circuit Description

The design of the dynamic compensator consists of CMOS pass gates that connect to integrated binary-weighted capacitors. In our design, we utilize three integrated capacitors that can be switched in (C_1, C_2 and C_3). This number can be increased, but our experiments indicate that sufficient resolution can be achieved using just three capacitors. Each of these capacitors use a pass gate to connect to the wire bond (Pass Gate #1, Pass Gate #2, Pass Gate #3). Each pass gate has a control signal which either connects / isolates the capacitors to / from the on-chip I/O pad, which is connected to one end of the wire bond. Figure 2 shows the schematic of the dynamic compensator design.

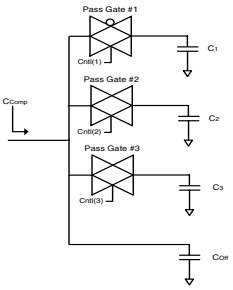

Fig. 2. Dynamic Compensator Circuit

B. Capacitor Design

The diffusion regions associated with the pass gates contribute an additional capacitance to C_{comp1}, which must be considered in the design. For each of the three programmable capacitor banks, the net capacitance will be the sum of the diffusion capacitance of the pass gate and the integrated capacitor. If the pass-gate of any bank i is turned off, then bank i simply contributes a capacitance C_{pgi} to C_{comp1}.

$$C_{Bank1} = C_{pg1} + C_1 \quad (8)$$

$$C_{Bank2} = C_{pg2} + C_2 \quad (9)$$

$$C_{Bank3} = C_{pg3} + C_3 \quad (10)$$

To achieve a programming range with uniform steps, the integrated capacitors are sized such that:

$$C_{Bank3} = 2 \cdot C_{Bank2} = 4 \cdot C_{Bank1}$$

Structure	$C_{density}$	$L_{density}$	Size	C_{total}	L_{total}	Z_0
Wire-Bond	26 fF/mm	569 pH/mm	1 mm	26 fF	0.569 nH	148 Ω
Wire-Bond	26 fF/mm	569 pH/mm	2 mm	52 fF	1.138 nH	148 Ω
Wire-Bond	26 fF/mm	569 pH/mm	3 mm	78 fF	1.707 nH	148 Ω
Wire-Bond	26 fF/mm	569 pH/mm	4 mm	104 fF	2.276 nH	148 Ω
Wire-Bond	26 fF/mm	569 pH/mm	5 mm	130 fF	2.845 nH	148 Ω
On-Chip MIM-Based Capacitor	1.15 fF/μ^2	negligible	100μ × 100μ	11.5 pF	negligible	N/A
On-Chip Device-Based Capacitor ($V_{GS} = 0v$)	2.7 fF/μ^2	negligible	100μ × 100μ	27 pF	negligible	N/A
On-Chip Device-Based Capacitor ($V_{GS} = 1.5v$)	13.8 fF/μ^2	negligible	100μ × 100μ	138 pF	negligible	N/A
On-Package Embedded Capacitor	420 fF/mm^2	238 fH/mm^2	0.5 mm x 0.5 mm	0.105 pF	59 fH	N/A

TABLE I

ELECTRICAL PARAMETERS FOR SYSTEM INTERCONNECT

Using three control bits, 8 programmable values of capacitance can be connected to the wire bond in increments of C_{Bank1}. The minimum capacitance value C_{min} of the compensator corresponds to the sum of the diffusion capacitances of the three pass-gates. Using the conventions just described, the range of the compensator can be described as:

$$C_{min} = C_{pg1} + C_{pg2} + C_{pg3} \tag{12}$$

$$C_{max} = C_{min} + C_{Bank1} + C_{Bank2} + C_{Bank3} \tag{13}$$

$$C_{step} = C_{Bank1} \tag{14}$$

In this work, the pass gates are implemented using a 0.1um CMOS process from BPTM [14], [16]. Just as in the case of the static compensator, the integrated capacitors (C_1,C_2, C_3, C_{min}) are implemented using two different on-chip techniques that are evaluated in this work (MIM-based and Device-Based). Both of these capacitor techniques are evaluated for range, area efficiency, and non-linearity for applicability in the dynamic compensator design.

C. Pass Gate Design

As described in the previous section, the pass gates will contribute to the total capacitance of each bank. The pass gates must be sized to have a sufficiently low impedance to drive the integrated capacitors (C_1, C_2, C_3). Typical CMOS circuit design rules dictate that the pass gate sizing will be 1/3 of the size of an equivalent inverter that represents the integrated capacitor being driven by the pass-gate[5]. This rule dictates the amount of capacitance that will be present in each bank due to the pass gate and to the integrated capacitor.

$$C_{pgi} = \frac{1}{3} \cdot C_{Banki} \tag{15}$$

$$C_i = \frac{2}{3} \cdot C_{Banki} \tag{16}$$

Using the equations 8-16 and the values from Table I , the sizing of the resulting compensation circuitry can be found. Table IV lists the values of the capacitors used in the dynamic compensator that will match the impedance of the wire bond to 50Ω (equation 3).

$Length_{wb}$	C_{comp1}
1 mm	202fF
2 mm	403fF
3 mm	605fF
4 mm	806fF
5 mm	1008fF

TABLE IV

DYNAMIC COMPENSATION CAPACITOR VALUES

Table V lists the device sizes of the dynamic compensator circuit. The capacitances C_1, C_2 and C_3 are implemented as square devices for a minimal area utilization. The total area of the compensator is the size of the equivalent enclosing square for the compensator. This equivalent square represents the *normalized* area for the circuitry. It is clear that the MIM-based dynamic compensator occupies more area than the Device-based compensator. However, the non-linearity of both compensators must be analyzed to compare the efficiency of the two circuits. In the next section, experimental results are presented that compare the functionality of the two compensator designs.

	MIM-Based	Device-Based
Component	Area (W × L)	Area (W × L)
Pass Gate #1	32.4μm x 0.1μm	32.4μm x 0.1μm
Pass Gate #2	62.5μm x 0.1μm	62.5μm x 0.1μm
Pass Gate #3	129.6μm x 0.1μm	129.6μm x 0.1μm
C_{off}	8.5μm x 8.5μm	2.5μm x 2.5μm
C_1	11μm x 11μm	3.3μm x 3.3μm
C_2	15.5μm x 15.5μm	4.6μm x 4.6μm
C_3	22μm x 22μm	6.6μm x 6.6μm
Total	65μm x 65μm	25μm x 25μm

TABLE V

DYNAMIC COMPENSATION CAPACITOR SIZES (NORMALIZED)

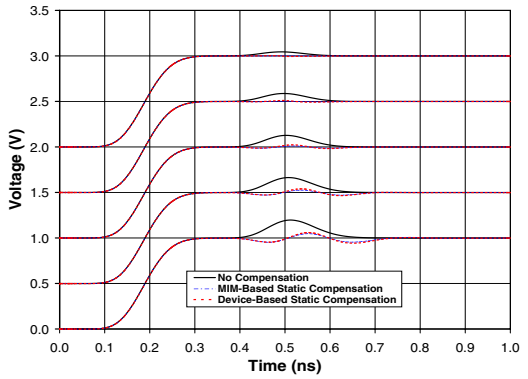

Fig. 3. Simulated TDR of Static Compensator

VII. EXPERIMENTAL RESULTS

To evaluate the compensator design, SPICE [13] simulations were conducted on the system.

A. Static Compensator Performance

In order to evaluate the performance of the static compensator, simulations were performed on all lengths of wire bonds listed in Table II. Figure 3 shows the simulated Time Domain Reflectrometry (TDR) waveforms of the static compensator (equation 2). A TDR waveform shows the magnitude of the reflection that is caused by the wire bond. For each length of wire bond (1mm to 5mm), a 117ps (3GHz) input step is used to stimulate the wire bond. In figure 3, the TDR waveforms are offset in the voltage axis (by 0.5V from each other) for viewability with the 1mm curve on the top and the 5mm curve on bottom. For each length of wire bond the non-compensated, MIM-based, and Device-based static compensation curves are shown. This figure shows the dramatic reduction in wire bond reflections when using a static compensator. Consider the TDR waveforms for the 5mm trace. The uncompensated waveform indicates that a large reflection is caused by the package and wire bond inductance. For the compensated TDR waveform, the effect of the reflection due to the package and wire bond inductance is dramatically reduced, allowing us to view the reflection due to the package capacitance (first negative dip in the TDR waveform) and the on-chip capacitance (the last dip in the TDR waveform). Table VI tabulates the reduction in reflections when using the static compensator(s).

Another means to evaluate the effectiveness of the compensator is to observe the input impedance of the structure in the frequency domain. Figure 4 shows the input impedance of the wire b versus frequency for the 3mm wire bond. In this figure,

$Length_{wb}$	$\Gamma_{No-Comp}$	$\Gamma_{MIM-Comp}$	$\Gamma_{Device-Comp}$
1 mm	4.5%	0.05%	0.5%
2 mm	8.7%	0.4%	1.2%
3 mm	12.7%	1.3%	2.4%
4 mm	16.4%	2.7%	4.1%
5 mm	19.8%	4.8%	6.0%

TABLE VI

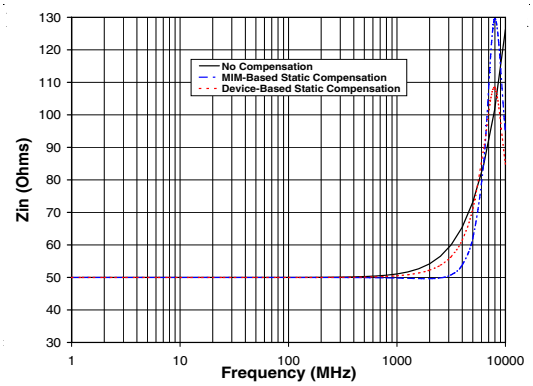

Fig. 4. Input Impedance of Static Compensator (3mm)

non-compensated, MIM-based, and Device-based static compensation curves. To compare their performance we record the frequency at which the input impedance changes by 10Ω from the design target of 50Ω. This figure illustrates that adding a static compensator can keep the lumped impedance of the wire bond closer to 50Ω up to a much higher frequency. In this case, the 3mm wire bond was kept to within 10Ω of the design target of 50Ω up to 4.8GHz when using the MIM-based compensator (compared to only 3.1GHz when considering the un-compensated wire bond).

Table VII lists the frequencies at which the input impedance strays to +/-10Ω from the design target for all the lengths of wire bonds evaluated.

$Length_{wb}$	$f_{No-Comp}$	$f_{MIM-Comp}$	$f_{Device-Comp}$
1 mm	9.3 GHz	14 GHz	12 GHz
2 mm	4.7 GHz	7.1 GHz	5.7 GHz
3 mm	3.1 GHz	4.8 GHz	3.8 GHz
4 mm	2.4 GHz	3.7 GHz	2.9 GHz
5 mm	1.9 GHz	3.0 GHz	2.5 GHz

TABLE VII

$f_{+/-10\Omega}$ FROM DESIGN (STATIC COMPENSATOR)

These results show the dramatic reduction in impedance mismatch when using a static compensator. In all cases, the MIM-based compensator outperformed the Device-based compensator.

B. Dynamic Compensator Performance

The same set of SPICE simulations were performed on the dynamic compensator to evaluate its performance.

1) Impedance Matching: Figure 5 shows the simulated TDR of the dynamic compensator (equation 2). Each length of wire bond (1mm to 5mm) is evaluated when stimulated with a 117ps (3GHz) input step. Again, the TDR waveforms are offset in the voltage axis (by 0.5V from each other) for view-ability with the 1mm curve on the top and the 5mm curve on bottom.

Table VIII tabulates the reduction in reflections when using the dynamic compensator(s), along with the binary setting used for the compensation.

Figure 6 shows the input impedance of the wire bond structure versus frequency for the 3mm wire bond using the dynamic compensator. Once again, adding a compensator can keep the lumped impedance of the wire bond closer to 50Ω up to a much higher frequency. In this case, the 3mm wire bond was kept to within 10Ω of the design target for up to 6.8GHz when using the Device-based compensator (compared to only 3.1GHz when considering the un-compensated wire bond).

$Length_{wb}$	$\Gamma_{No-Comp}$	$\Gamma_{MIM-Comp}$	$\Gamma_{Device-Comp}$	Setting
1 mm	4.5%	1.0%	1.0%	001
2 mm	8.7%	1.8%	1.3%	011
3 mm	12.7%	3.6%	3.0%	100
4 mm	16.4%	4.3%	3.3%	110
5 mm	19.8%	6.0%	5.0%	111

TABLE VIII

REFLECTION REDUCTION DUE TO DYNAMIC COMPENSATOR

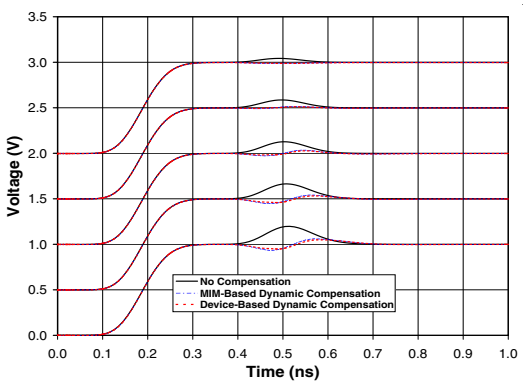

Fig. 5. Simulated TDR of Dynamic Compensator

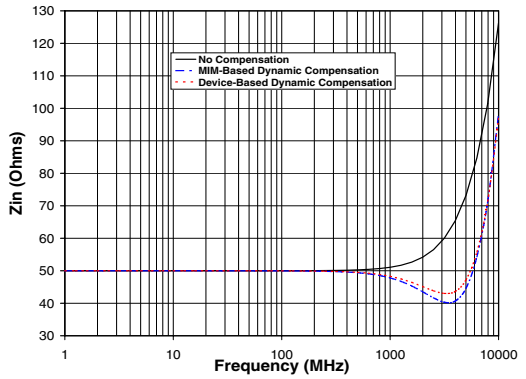

Fig. 6. Input Impedance of Dynamic Compensator (3mm)

Table IX lists the maximum frequencies for which the impedance was within +/- 10Ω of the 50Ω target, for all of the lengths of wire bonds evaluated using the dynamic compensator.

$Length_{wb}$	$f_{No-Comp}$	$f_{MIM-Comp}$	$f_{Device-Comp}$
1 mm	9.3 GHz	20 GHz	20 GHz
2 mm	4.7 GHz	10.1 GHz	10 GHz
3 mm	3.1 GHz	6.8 GHz	6.7 GHz
4 mm	2.4 GHz	5.2 GHz	5.1 GHz
5 mm	1.9 GHz	4.2 GHz	4.1 GHz

TABLE IX

$f_{+/-10\Omega}$ FROM DESIGN (DYNAMIC COMPENSATOR)

2) Compensator Range and Linearity: Due to the non-linearity of the Device-based capacitors and active pass gates, the linearity of the dynamic compensator was evaluated to ensure the desired range was being reached. For each dynamic compensator setting, the bias voltage was changed for $V_G = 0v$ to $V_G = 1.5v$ and the corresponding capacitance was recorded. Table X lists the effect of bias voltage on both the MIM-based and Device-based compensator circuits. This table clearly shows the non-linearity of the Device-based compensator which experiences as much as 33% capacitance variation when programmed to its maximum setting. This variation matches expected variation of CMOS polysilicon gate capacitors [5]. Note that the MIM capacitors also exhibit variability, which occurs due to the bias dependence of the pass gate diffusion capacitances [17]. While both dynamic circuits experience some bias voltage dependence, the compensators had sufficient range to cover wire bond lengths from 1mm to 5mm.

These results illustrate that the Device-based compensator outperformed the MIM-based compensator when implemented in a dynamic architecture. Also, both dynamic compensators outperform

		MIM-Based Compensator			Device-Based Compensator		
Compensator Setting	$C_{(desired)}$	$C_{(V_{bias}=0v)}$	$C_{(V_{bias}=1.5v)}$	$C_{average}$	$C_{(V_{bias}=0v)}$	$C_{(V_{bias}=1.5v)}$	$C_{average}$
001	200 fF	252 fF	262 fF	257 fF	222 fF	281 fF	251 fF
010	325 fF	373 fF	382 fF	378 fF	318 fF	414 fF	366 fF
011	450 fF	499 fF	540 fF	519 fF	423 fF	587 fF	505 fF
100	575 fF	588 fF	596 fF	592 fF	485 fF	651 fF	568 fF
101	700 fF	713 fF	754 fF	734 fF	592 fF	816 fF	704 fF
110	825 fF	828 fF	895 fF	862 fF	688 fF	968 fF	828 fF
111	950 fF	948 fF	1041 fF	994 fF	788 fF	1180 fF	984 fF

TABLE X

DYNAMIC COMPENSATOR RANGE AND LINEARITY

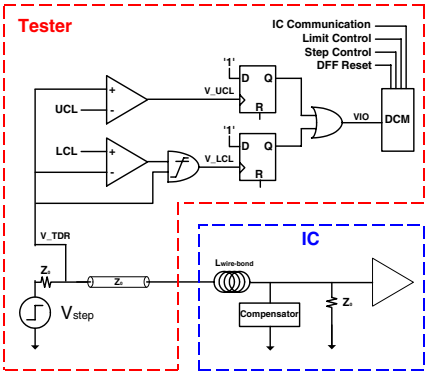

Fig. 7. Dynamic Compensator Calibration Circuit

3) Compensator Calibration: The circuit used to perform the calibration is inspired by TDR ideas, but is simplified for applicability in a standard, low-cost VLSI tester setting. The calibration circuitry is simple and can be placed in the IC test equipment so that extra circuitry is not needed on the IC. In addition, pre-existing control logic and software interfaces in the tester are used for calibration. Figure 7 shows the calibration circuitry for the compensator.

To measure the impedance discontinuity from the wire-bond / compensator, the IC tester transmits a voltage step into the IC package. The magnitude of the reflection from the discontinuity is measured in the tester using comparator circuits. The comparator circuits are used instead of a standard A/D converter (as in a true TDR system) to reduce complexity and cost. One comparator monitors for reflections that exceed a user-defined Upper Control Limit (UCL). A second comparator monitors for reflections that exceed a Lower Control Limit (LCL). The programmable voltages are set by a Digital Control Monitor (DCM) in the IC tester.

When a reflection from the wire-bond/compensator element is above/below the violation limits, the comparator(s) will output a glitch signal that indicates a limit violation (V_UCL / V_LCL). The limit violation glitch is fed into the clock input of a D-flip-flop whose data input is tied to a logic 1. The D-flip-flop serves as a trigger element that will switch and remain high when it observes any glitch from the comparators. The D-flip-flop will remain high until reset by the DCM. The output of the two D-flip-flops are fed into an OR-gate to combine the upper and lower violation signals into one input (VIO) that is monitored by the DCM.

When the DCM observes a violation, it will communicate with the IC under test to change the compensator settings. This can be achieved by using on-chip flash type non-volatile memory. Once the compensator is adjusted, the D-flip-flops are reset and another voltage step is launched into the IC package. This process is repeated until the magnitude of the reflections are within the LCL and UCL limits.

The lower control limit violation signal (V_LCL) is qualified using an AND-gate. The purpose of the AND-gate is to prevent glitches on V_LCL when the step voltage is below the LCL due to normal operating conditions such as the beginning of the rising edge of the step. The AND-gate is designed to have a high switch-point such that $V_{switchpoint-AND} >$ LCL. Once the step voltage exceeds the switch-point of the AND-gate, the glitches from the comparator are allowed to pass through to the D-flip-flop. Spurious glitches which may be observed when the step voltage is below the AND gate switch-point are thus filtered out, and the glitches at the output of the AND gate will therefore be solely due to reflections from the package (which violate the LCL).

VIII. CONCLUSION

In this paper, we present the design of two compensation circuits for use in matching the impedance of wire bonds to the target characteristic impedance of the board / package interconnect. The compensators placed capacitances near the wire bond to reduce the impedance of the wire bond structure. Our static compensator placed pre-determined capacitances on both the package and the on-chip I/O pad, to surround the wire bond inductance. Our dynamic compensator placed programmable capacitances on-chip. These can be changed to accommodate varying lengths of wire bonds. For both compensators, two types of on-chip capacitors were explored (MIM-based and Device-based).

Both compensators significantly reduced the reflections due to the wire bond impedance discontinuity. In the case of the static compensator, the MIM-based on-chip capacitors outperformed the Device-based capacitors. In the case of the dynamic compensator, the Device-based on-chip capacitors outperformed the MIM-based. All compensators could be implemented in less area than a traditional wire bond pad, making them ideal for implementation directly beneath the pad structure.

The dynamic compensator outperformed the static compensator in all respects. The dynamic compensator was able to bound reflections to $<5\%$ for wire bond lengths up to 5mm (compared to as much as 20% for an uncompensated 5mm wire bond). In addition, the dynamic compensator held the input impedance to within 10Ω of the target impedance (50Ω) up to 6.8 GHz compared to only 3.1 GHz for an uncompensated 3mm wire bond.

The compensators presented in this paper can be used to increase the throughput of wire bond packaging technologies as data rates increase. This technique will aid in keeping the cost of VLSI packaging down while still addressing the need for increased system performance.

REFERENCES

[1] R. Tummalo, *Fundamentals of Microsystem Packaging*. McGraw-Hill, 2001.

[2] J.M. Hobbs, H. Windlass, V. Sundaram, S. Chun, G.E. White, M. Swaminathan, R.R. Tummala, "Simultaneous switching noise suppression for high speed systems using embedded decoupling," *Electronic Components and Technology Conference, 2001. Proceedings. 51st*, pp. 339–343, June 2001.

[3] Kuo-Yu Chou, Ming-Jer Chen, "Active circuits under wire bonding I/O pads in 0.13 m eight-level Cu metal, FSG low-k inter-metal dielectric CMOS technology," *Electron Device Letters, IEEE*, pp. 466–468, Oct 2001.

[4] J. Prasad, M. Anser, M. Thomason, "Electrical characterization of dielectrics (oxide, nitride, oxy-nitride) for use in MIM capacitors for mixed signal applications," *Semiconductor Device Research Symposium, 2003 International*, pp. 326–327, Dec 2003.

[5] Y. L. S.M. Kang, *CMOS Digital Integrated Circuits*. McGraw-Hill, 1999.

[6] H. Johnson and M. Graham, *High-Speed Signal Propagation*. Prentice Hall PTR, 2003.

[7] H. Kim, B.K Sun, J. Kim, "Suppression of GHz range power/ground inductive impedance and simultaneous switching noise using embedded film capacitors in multilayer packages and PCBs," *Microwave and Wireless Components Letters, IEEE*, vol. 14, pp. 71–73, Feb 2004.

[8] H. Kim, Y. Jeong, J. Park, S. Lee, J. Hong, "Significant reduction of power/ground inductive impedance and simultaneous switching noise by using embedded film capacitor," *Electrical Performance of Electronic Packaging*, pp. 129–132, Oct 2003.

[9] D. Balaraman, J. Choi, V. Patel, P.M. Raj, I.R. Abothu, S. Bhattacharya, L. Wan, M. Swaminathan, R. Tunimala, "Simultaneous switching noise suppression using hydrothermal barium titanate thin film capacitors," *Electronic Components and Technology, 2004. ECTC '04. Proceedings*, pp. 282–288, June 2004.

[10] J.H. Ahm, K.T. Lee, M.K. Jung, Y.J. Lee, B.J. Oh, S.H. Liu, Y.H. Kim, Y.W. Kim, K.P. Suh, "Integration of MIM capacitors with low-k/Cu process for 90 nm analog circuit applications," *Interconnect Technology Conference, 2003. Proceedings of the IEEE 2003 International*, pp. 183–185, June 2003.

[11] W. Dally and J. Poulton, *Digital Systems Engineering*. Cambridge, U.K.: Cambridge University Press, 1998.

[12] "Raphael." http://www.synopsys.com/products/mixedsignal/ raphael_ds.html. Synopsys Inc.

[13] L. Nagel, "SPICE: A Computer Program to Simulate Computer Circuits," in *University of California, Berkeley UCB/ERL Memo M520*, May 1995.

[14] "BSIM3 Homepage." http://www-device.eecs.berkeley.edu/~bsim3/.

[15] "BPTM Homepage." www-device.eecs.berkeley.edu/~ptm/.

[16] Y. Cao, T. Sato, D. Sylvester, M. Orshansky, and C. Hu, "New paradigm of predictive MOSFET and interconnect modeling for early circuit design," in *Proc. of IEEE Custom Integrated Circuit Conference*, pp. 201–204, Jun 2000. http://www-device.eecs.berkeley.edu/ ptm.

[17] "BSIM3 Manual, Chapter 4." http://www-device.eecs.berkeley.edu/~bsim3/ ftpv322/Mod_doc/V322manu.tar.Z.